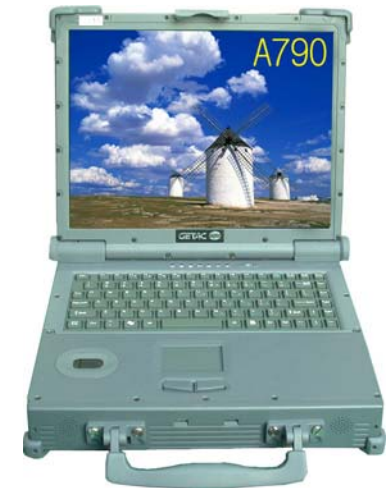


SERVICE MANUAL FOR

A790



BY: Irene Yu

Validation Tool Research Department/EDVD

Mar. 2007



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1. Hardware Engineering Specification

1.1 Introduction

1.1.1 General Description

This document describes the system hardware engineering specification for A790 portable notebook computer system. The A790 notebook computer is a new mainstream high performance thin and light notebook in the MiTAC notebook family.

1.1.2 System Overview – Marketing Requirement

The new A790 is ruggedized notebook, high-portability industrial computer. It can be used in the vehicle, field, and office. The notebook computer also can connect with a docking to extend the capability of I/O devices.

The Intel 945GME North Bridge chipset supports Host system bus at 667MHz, 2 slots of SODIMM (400/533/667 MHz) 256MB to 2GB total, Internal Video controller support RGB, DVO and LVDS video interfaces and Hub interface to South Bridge-ICH7-M.

The Intel 82801GBM(ICH7-M) South Bridge supports PCI 2.2 33MHz, Integrated IDE controller, Integrated USB hub 2.0 up to 8 ports, Azalia interface (for audio and line modem), LPC interface, SMBus 1.1 interface and power management with ACPI 2.0.

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On PCI Bus interface exist PCI1520 card-bus controller supports PCMCIA and Card-Bus, Wireless LAN on mini PCI, PCI Expansion interface, Bay2 option interface and PCI to ISA Bridge.

On LPC interface exist SUPER I/O that is SIO10N268 and connected the Keyboard embedded controller H8S/2140 and Flash memory for BIOS. SIO10N268 provides 1 parallel, IrDA, 1 Serial ports and ISA Bridge.

There are two SMBUS interfaces; one is connect from ICH7-M and operating under master mode, the second is multi-master Bus and connected from H8S/2140.

The master provides interface to Synthesizer and to memory identification.

The multi-master channel used for Thermal sensor controller and G-sensor controller.

A codec (ALC260) with TI audio amplifier stereo analog audio to internal speakers, audio Jack and docking. digital audio- SPDIF standard also provided to audio Jack and to docking. Internal line modem module – ASKEY-V1456VQL-7 will be used.

System also provides LEDs to display system status, such as Power On, Battery state, HDD, Num Lock, Caps Lock and Scroll Lock.

The system also provides a port to expand Docking capability. Input/output (I/O) ports can include parallel port, serial port, VGA port, USB.

The system also provides DVD-ROM, Bluetooth, Fingerprint reader, GPS, GPRS,CDMA.

A full set of software drivers and utilities are available to allow advanced operating systems such as Windows 2000 and Windows XP to take full advantage of the hardware capabilities.

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1.2 System Hardware Parts-1

CPU	Intel Yonah Processor Dual Core Low Voltage 1.66 GHz (Processor Number:x48) in uFC-BGA package without CPU socket FSB 667 MHz CPU Thermal ceiling: 15 W
Core logic	Intel 945GM (Calistoga) Chipset + ICH7-M
L2 Cache	On-die 2 MB L2 Cache
Structure	3-spindle
Display	12.1"/14.1" TFT XGA LCD resolution: 1024x768- • SPWG type • Factory optional 14.1" TFT SXGA+ (1400x1050) & SXGA • Factory optional 12.1" Touch Screen; • Factory optional Sunlight readable type LCD • Factory optional 17" LCD Wide- (Make new tooling only for A,B part ; C, D part only could be modified by after die-casting)
System BIOS	1MB Flash EEPROM • Includes System BIOS, VGA BIOS, plug & play, and ACPI 2.0 capability • Boot from IDE and USB and PCMCIA devices • Suspend to DRAM/HDD • PC2001 compliance • Support G-sensor
Memory	Two 200-pin SO-DIMMS socket for memory expansion Support DDR2 400/533MHz Max: 2 GB

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1.2 System Hardware Parts-2

VGA Controller	Integrated in 945GM chipset, Intel® GMA 950 graphics controller; Integrated 32-bit 3D/2D gfx core with Dynamic Video Memory Technology • Support DirectX® 9.0 • Support PCI Express x16 Graphics • Dual View Function • LCD/CRT simultaneous display capability Factory Optional ATI M54-CSP VGA controller with 128MB memory
Video Memory	Standard: Shared system memory 64MB
Audio	Azalia 32 bits 192 KHz • Built-in 2 speakers 2W • Built-in Mic and Line-Out connector
HDD	Rugged and removable HDD; support Ultra DMA 100 / SATA 160 (Factory Optional) 2.5" 9.5mm height; 60GB, 80 GB, 100GB or above Built-in G-sensor to prevent HDD from physical damage during drop Factory Option: HDD heater for low temperature (-20°C) support Optional Low Temperature HDD Optional Flash HDD
Keyboard	• Shower-proof and dust-proof rubber Keyboard • Optional LED Back-Light Rubber Keyboard
Pointing Device	• A touch-sensitive control pad with Microsoft Win Mouse function coexist • Factory optional support Glove Used Touch Pad
Bay-1 Modules	Removable for CD-ROM, DVD-Dual, FDD, Bay1 Battery, 2 nd HDD (Compatible to A770's Bay1 options)

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1.2 System Hardware Parts-3

Bay-2 Modules	• 2nd PCMCIA – Removable Type III×1 or Type II×2 Module • COM Port Module - RS-232, 422 Module • GPS Module • GPRS/GSM Module • GPS + GPRS/GSM Modules + Bluetooth class1 (V1.2; class 1) • Ultra 320 SCSI Module • Bay2 Li-Ion Battery Pack • Bay2 FDD (Compatible to all above A770's Bay2 options) • New Wireless Modem (CDMA:EVDO) • Hot swappable 3rd HDD (USB to IDE) • Smart card reader • PCI express bus support (Factory option)
I/O Port	• Serial port × 1 • Parallel port (EPP/ECP) × 1 • RJ-11 × 1 • RJ-45 × 1 • VGA monitor port × 1 • USB2.0 × 2 • DC input × 1 • IrDA port × 1 • Port Replicator port × 1 • IEEE 1394 B Port × 1 (Compatible to 1394A , by cable) • Mic-In and Line-Out • Factory optional fingerprint recognition x 1 (On C-part)

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1.2 System Hardware Parts-4

PCMCIA Card	• Type III×1 or Type II ×2 in Bay1 • Card Bus compatible
Battery	Smart battery; KBC BIOS controllable Primary Li-Ion Type without 2 nd Battery for 6 hours Bay1 Li-Ion Smart Battery for 2.5 hours Bay2 Li-Ion Smart Battery for 2.5 hours (Without discrete VGA)
AC adapter	Universal AC adapter -Input: 100-240v, 50/60Hz AC
Communication	Standard • 10/100/1000 Base-T LAN (Reserve for TPM security function) • 56K, V92. Modem Factory optional • 802.11a/b/g Wireless LAN (Intel 3945ABG) • Bluetooth (V1.2; class1) in Bay2 • Wireless Modem in Bay-2(GPRS/GSM, CDMA)
Cooling	Fan less
Security	Kensington Lock Slot
Dimensions	12.1" version: 315(W)x255(D)x70(H) mm; 14.1" version: 315(W)x265(D)x70(H) mm ; 17" version: 410(W)x296(D)x70(H)
Weight	12.1" version: Under 5.9 Kg (12.9 lbs); 14.1" version: Under 6Kg 17" version: Under 8.5Kg
Software	Support Windows 2000 / Windows XP / Linux /Windows NT/Windows

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1.2 System Hardware Parts-5

Peripheral	• New Expansion unit (2 PCI slots) • New expansion unit (2 PCI express slots) • Port replicator (SIOx2, PIOx1, USBx4, VGAx1, DC input, Power • External 3-pcs battery charger • 12-32VDC car adapter • New Carrying Bag • Shock Mount • Ultra Shock Mount • Vehicle Mount / Docking • USB external FDD (Compatible to all A770's Peripheral options except expansion unit)
Regulation	FCC part 15, Subpart B, Class B, UL, CUL, TUV, CE, CCC, WHQL, BSMI, Optional MIL-STD-461E , E-mark , Explosive CSA C1D2
Environmental Standard (Main System)	
Enclosure	According to IEC529 IP54, MIL-STD-810F, 506.4 Procedure III-drip
Drop	According to IEC68-2-32/MIL-STD-810F, 516.5 26 times 3 feet height free drop onto wood (Only for 12.1'' and 14.1'')
Temperature	According to IEC68-2-1,2,14/MIL-STD-810, Method 501.4,502.4 Operating: Standard: 0°C to 60°C (Allow system degrade at high temperature environment) Optional: -20°C to 60°C(with HDD heater) Non Operating: -40°C to 70°C
Shock	According to IEC68-2-27/MIL-STD-810F,516.5 Operating: 15g, 11ms, half sine wave. Non-operating: 50g,11ms,halfsine wave.

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1.2 System Hardware Parts-6

Vibration	According to IEC68-2-6 Sinusoidal Wave Vibration: Operating: 10~500Hz, 0.075mm/1.0g Non-operating: 10~500Hz, 0.150mm/2.0g Random Vibration: Operating: MIL-STD-810F, 514.5C-1 high way truck vibration exposure Non-operating: MIL-STD-810F, 514.5C-17 General minimum integrity exposure
Humidity	According to IEC68-2-30/MIL-STD-810F,507.4 5% to 95% RH, non-condensing.
Altitude	According to IEC68-2-13/MIL-STD-810F,500.4 Operating: 15,000ft Non-operating: 40,000ft Altitude change rate: 2000ft/min
ESD	According to IEC1000-4-2 Air Discharge: 0KV~8KV(included), no any error 8KV~15KV, allow soft error Contact Discharge: 0KV~4KV(included), no any error 4KV~8KV, allow soft error

Standard Configuration	Yonah LV 1.66G(x48) Without Discrete VGA Without HDD Encryption
With discrete VGA Option Bundle Configuration	Yonah LV 1.66G(x48) With discrete VGA ATI M54-CSP128MB

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1.3 Function Description

1.3.1 CPU – Intel Yonah

- First dual core processor for mobile (Yonah and Yonah Low Voltage skus)
- 667 MT/s (667 MHz) FSB support
- On-die primary 32-KB instruction cache and 32KB write-back data cache
- On-die,2-MB second level cache with Advanced Transfer Cache Architecture shared between the two cores
- Streaming SIMD Extensions 2 (SSE2) and Streaming SIMD Extensions 3 (SSE3)
- Supports Intel Architecture with Dynamic Execution
- Advanced gunning transceiver logic (AGTL+) bus driver technology
- Enhanced Intel SpeedStep technology to enable real-time dynamic switching between multiple voltage and frequency points
- Data Prefetch Logic
- 479-ball Micro-FCBGA packages

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1.3.2 North Bridge & 3D Graphics DDR2 Chipset– Intel 945GM

FSB Support

- AGTL + bus driver technology with integrated GTL termination resistor (gated AGTL+ receivers for reduced power)
- Supports 32-bit AGTL + host bus addressing
- 667MT/S (667 MHz) and 533 MT/s (533 MHz) FSB support
- 2X address, 4X data
- Host bus dynamic bus inversion HDINV support
- 12 deep, in – order queue

External Graphics Using PCI Express Architecture Interface

- One×16 (16 lanes) PCI Express port intended for graphics attach; fully compliant to the PCI Express Base Specification revision 1.0a
- Maximum theoretical realized bandwidth on interface of 4GB/s in each direction simultaneously, for an aggregate of 8GB/s when ×16

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- Automatic discovery, negotiation, and training of link out of set
- Supports traditional PCI style traffic (asynchronous snooped, PCI ordering)
- Supports traditional AGP style traffic (asynchronous non-snooped, PCI-X ordering)
- Hierarchical PCI –compliant configuration mechanism for downstream devices (i.e. normal PCI 2.3 Configuration space as a PCI-to-PCI bridge)
- Supports Lane Reversal and Bit Swapping

Integrated System Memory DRAM Controller

- Supports up to two DDR2 SDRAM channels (64 bit wide per channel)
- One SO-DIMM connector per channel
- Maximum of two, double-sided unbuffered SO-DIMMs (4 rows populated)
- Minimum amount of memory supported is 128 MB ($16 \text{ MB} \times 16\text{-b} \times 4 \text{ devices} \times 1 \text{ rows} = 128 \text{ MB}$) using 256 MB technology
- 256 MB, 512 MB and 1 GB technology using $\times 8$ and $\times 16$ devices
- Three memory channel organization are supported for DDR2
 - Single channel

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- Dual channel symmetric
- Dual channel asymmetric
- Outputs may be disabled via SMBus
 - Supports on-die termination (ODT) for DDR2
- Supports Fast Chip Select mode
- Supports partial writes to memory using Data Mask signals (DM)
- Supports high-density memory package for DDR2 type devices
- Supports Reduced Power DDR2 (RPDDR2)
- Supports Intel Rapid Memory Power Management

Internal Graphics Controller

- Graphics Core Frequency
 - 2D Display core frequency at 133, 200 or 250 MHz @ Vcc=1.05 V depending on the host/ memory configurations
 - 3D Render core frequency at 133, 166, 250 MHz @Vcc=1.05 V depending on the host/ memory configurations
 - Intel® Smart 2D Display Technology

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- Intel® Dual-Frequency Graphics Technology support
- Dynamic Video Memory Technology (DVMT) 3.0 support
- 3D Graphics Core Frequency
 - DirectX* 9.0 support
 - OpenGL* 1.5 and 2.0 support
 - Zone rendering 2.0 support
- Analog CRT DAC Interface Support
 - Supports max DAC frequency up to 400 MHz
 - 24-bit RAMDAC support
 - DDC2B compliant
 - Up to 2048 x 1536 resolution support
- Analog TV-Out Interface Support
 - Integrated TV-Out device supported on display pipes A and B
 - NTSC/PAL encoder standard formats supports
 - 480 i/480 p/576 i/576 p/720 p/1080 i/1080 p modes supported
 - Tri-level Sync signal
 - Multiplexed output interface

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- Composite video with S-Video
- S-Video
- Component video
- Up to 1024 x 768 resolution supported for NTSC/PAL
- Macrovision, oversean scaling, and flicker filtering support
- Serial digital video out Port (SDVO) interface support
 - Two SDVO ports are muxed with a subset of the external graphics interface using PCI Express Architecture signals
 - Each SDVO port support display pixel rates up to 200 MP/s (600 MB/s)
 - Supports a variety display devices such as DVI, TV-Out, LVDS, Etc
 - Supports hot plug and display
 - Support for HDCP SDVO devices
 - Support for Macrovision on SDVO TV-Out devices
 - Support for Lane Reversal
- Digital LVDS Interface Support
 - Integrated dual channel LVDS interface supported on display pipe B only
 - Compliant with ANSI/TIA/EIA –644-2001 spec

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- Supports 25 MHz to 112MHz single/dual channel LVDS LCD interface with support for following format of
 - 1 x 18 bpp for TFT panels with single channel LVDS
 - 2 x 18 bpp for TFT panels with dual channels LVDS
 - Panel Fitting, Panning, and Center mode supported
 - Spread spectrum clocking (SSC) supported
 - Panel Power Sequencing compliant with SPWG timing specification
 - Integrated PWM or dedicated GMBus interface for LCD backlight inverter control
 - Intel® Display Power Savings Technology 2.0 support
 - Maximum UXGA panel size supported
 - Maximum WUXGA wide panel size supported
- PCI Express x1 Port Support
 - One general purpose PCI Express port support
 - External graphics using PCI Express architecture and SDVO are functional in this mode
- Direct Media Interface (DMI)
 - Chip-to-chip interconnect between the GMCH and Intel 82801 GBM
 - DMI x2 and DMI x4 configurations support
 - Bit swapping is supported

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- Lane reversal is supported
- Packing/Power
 - 1466-ball micro-FCBGA (37.5 mm x 37.5 mm) with a 42-mil x 34-mil ball pitch
 - VCC (1.05 core supply)
 - VCCSM (DDR2=1.8 V I/O supply)
 - VCC3G (1.5 V PIC-E/DMI analog supply). VCC3A_GBG(2.5V PCI-E/DMI band gap supply)
 - VCCA_HPLL (1.5 V host VCO supply), VCCA_MPLL (1.5 V system memory VCO)
 - VCCD_HMPLL (1.5 V digital dividers supply). VCCA_3GPLL (1.5 V PCI-E PLL supply)
 - VCCA_DPLLA (1.5 V Display A PLL supply), VCCA_DPLLB (1.5 V Display B PLL supply)
 - VCCHV (3.3 V high voltage supply), VCCA_CRTDAC (2.5 V CRT analog supply)
 - VCC_SYNC (2.5 V HSYNC/VSYSNC supply)
 - VCCD LVDS (1.5 V digital supply), VCCTX_LVDS (2.5 V Data/CLK Tx power supply)
 - VCCA_LVDS (2.5 V LVDS analog supply)
 - VCCA_TVBG (3.3 V TV DAC band gap supply), VCCD_TVDAC (1.5 V TV DAC supply)
 - VCCDQ_TVDAC (1.5 V TV DAC quiet supply), VCCA_TVDACA (3.3 V TV-Out Channel A supply), VCCA_TVDACB (3.3 V TV-Out Channel B supply). VCCA_TVDACC (3.3 V TV-Out Channel C supply)

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1.3.3 System Frequency Synthesizer- ICS9LPR310

- ICS9LPR310 is a low power CK410M-compliant clock specification. This clock synthesizer provides a single chip solution for next generation P4 Intel processors and Intel chipsets. ICS9LPR310 is driven with a 14.318 MHz crystal
- Supports tight ppm accuracy clocks for Serial-ATA and PCIEX
- Supports programmable spread percentage and frequency
- Uses external 14.318 MHz crystal, external crystal load caps are required for frequency tuning
- PEREQ# pins to support PCIEX power management
- Programmable watchdog safe frequency
- Low power differential clock outputs (No 50ohm resistor to GND needed)

1.3.4 PCMCIA Controller- TI PCI 1520 + TPS2224A

TI PCI 1520 - Cardbus Controller

- The PCI1520, a dual-slot CardBus controller designed to meet the PCI Bus Power Management Interface Specification for PCI to CardBus Bridges, is an ultralow power high-performance PCI-to-CardBus control

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that supports two independent card sockets compliant with the PC Card Standard

- The PCI1520 provides features that make it the best choice for bridging between PCI and PC Cards in both notebook and desktop computers. The 1997 PC Card Standard retains the 16-bit PC Card specification defined in PCI Local Bus Specification and defines the new 32-bit PC Card, CardBus, capable of full 32-bit data transfers at 33 MHz. The PCI1520 supports any combination of 16-bit and CardBus PC Cards in the two sockets, powered at 5 V or 3.3 V, as required
- The PCI1520 is compliant with the PCI Local Bus Specification, and its PCI interface can act as either a PCI master device or a PCI slave device. The PCI bus mastering is initiated during CardBus PC Card bridging transactions. The PCI1520 is also compliant with PCI Bus Power Management Interface Specification
- Key Features
 - 209-terminal MicroStar BGA ball-grid array (GHK/ZHK) package
 - 2.5 V core logic and 3.3 V I/O with universal PCI interfaces compatible with 3.3 V 5 V PCI signaling environments
 - Integrated low-dropout voltage regulator (LDO-VR) eliminates the need for an external 2.5 V power supply
 - Mix-and-match 5-V/3.3-V 16-bit PC Cards and 3.3-V CardBus Cards
 - Two PC Card or CardBus slots with hot insertion and removal

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- Serial interface to TITPS222X dual-slot PC Card power switch
- Burst transfers to maximize data throughput with CardBus Cards
- Interrupt configurations: parallel PCI, serialized PCI, parallel ISA, and serialized ISA
- Serial EEPROM interface for loading subsystem ID and subsystem vendor ID
- Pipelined architecture for greater than 130-Mbps throughput from CardBus-to-PCI and from PCI-to-Card Bus

TPS2224A - PCMCIA and CardBus Power Switch

- The TPS2224A Card Bus power-interface switch provide an integrated power management solution for two PC Card sockets. These devices allow the controlled distribution of 3.3 V, 5 V, 12 V to each card slot. The current-limiting and thermal protection features eliminate the need for fuses. Current-limiting reporting helps the user isolate a system fault. The switch Rds(on) and current-limiting values have been set for the peak and average current requirements stated in the PC Card specification
- Key Features
 - Fast Current Limit Response Time
 - Fully Integrated VCC and VPP Switching for 3.3 V, 5 V, and 12 V
 - Meets Current PC Card Standards
 - VPP Output Selection Independent of VCC

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- 12 V and 5 V Supplies Can Be Disabled
- TTL-Logic Compatible Inputs
- Short-Circuit and Thermal Protection
- 140 A (Typical) Quiescent Current from 3.3 V Input
- Break-Before-Make Switching
- Power-On
- Reset 40 to 85 Operating Ambient Temperature Range
- 32-Pin SSOP Package

1.3.5 Read Only Memory (Flash Rom)

- FWH bus interface
- Single 3.3 V-operations
 - 3.3 V-volt Read
 - 3.3 V-volt Erase
 - 3.3 V-program
- Fast program operation
 - VPP=12 V

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- Byte-by-Byte programming: 9 s (typ.)
- Fast erase operation
- Sector erase 0.9 Sec. (typ.)
- Fast read access time : T_{kg} 11ns
- Endurance: 30 K cycles (typ.)
- Twenty-year data retention
- 16 Even sectors with 64 K bytes
- Any individual sector can be erased
- Dual BIOS function
 - Full-chip partition with 8 M-bit or dual-block partition with 4 M-bit
- Hardware protection
 - #TBL supports 64-Kbyte Boot Block hardware protection
 - #WP supports the whole chip except Boot Block hardware protection
- Hardware Features
- Ready/#Busy output(RY/#BY)

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- Detect program or erase cycle completion
- Hardware reset pin (#RESET)
 - Reset the internal state machine to the read mode
- VPP input pin
 - Acceleration (ACC) function accelerates program timing
- Low power consumption
 - Read Active current: 15 mA (typ. for FWH mode)
- Automatic program and erase timing with internal VPP generation
- End of program or erase detection
 - Toggle bit
 - Data polling
- Latched address and data
- TTL compatible I/O
- Available packages: 32 L PLCC, 32 L STSOP, 40 L TSOP(10×20 mm), 32 PLCC Lead free, 32 L STSOP Lead free and 40 L TSOP(10×20 mm) Lead free

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1.3.6 Keyboard Controller

- The H8S/2140B is a high-speed central processing unit with an internal 32-bit architecture that is upward-compatible with the H8/300 and H8/300H CPUs. The H8S/2000 CPU has sixteen 16-bit general registers, can address a 16-Mbyte linear address space, and is ideal for real-time control

Detail specification as below

- Bus Controller
 - Basic bus interface
 - Burst ROM interface
 - Idle cycle insertion
 - Bus arbitration function
- Data Transfer Controller
- Programmable watchdog safe frequency
 - Transfer is possible over any number of channels
 - Three transfer modes
 - One activation source can trigger a number of data transfers (chain transfer)

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- Direct specification of 16-Mbyte address space is possible
- Activation by software is possible
- Transfer can be set in byte or word units
- A CPU interrupt can be requested for the interrupt that activated the DTC
- Module stop mode can be set
- 16-Bit Free-Running Timer (FRT)
 - Selection of four clock sources
 - Two independent comparators
 - Four independent input capture channels
 - Counter clearing
 - Seven independent interrupts
 - Special functions provided by automatic addition function
- 8-Bit PWM Timer (PWM)
 - Operable at a maximum carrier frequency of 625 kHz using pulse division (at 10 MHz operation)
 - Duty cycles from 0 to 100% with 1/256 resolution (100% duty realized by port output)
 - Direct or inverted PWM output, and PWM output enable/disable control
- 14-Bit PWM Timer (PWMX)

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- Division of pulse into multiple base cycles to reduce ripple
- Two resolution settings
- Two base cycle settings
- Four operating speeds
- Four operation clocks (by combination of two resolution settings and two base cycle settings)
- 8-Bit Timer (TMR)
 - Selection of clock sources
 - Selection of three ways to clear the counters
 - Timer output controlled by two compare-match signals
 - Cascading of TMR_0 and TMR_1
 - Multiple interrupt sources for each channel
- Timer Connection
 - Five input pins and four output pins, all of which can be designated for phase inversion
 - An edge-detection circuit is connected to the input pins, simplifying signal input detection
 - TMR_X can be used for PWM input signal decoding
 - TMR_X can be used for clamp waveform generation
- Watchdog Timer (WDT)
 - Selectable from eight (WDT_0) or 16 (WDT_1) counter input clocks

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- Switchable between watchdog timer mode and interval timer mode
- Serial Communication Interface (SCI & IrDA)
 - Choice of asynchronous or clocked synchronous serial communication mode
 - Full-duplex communication capability
 - The on-chip baud rate generator allows any bit rate to be selected
 - Choice of LSB-first or MSB-first transfer (except in the case of asynchronous mode 7-bit data)
 - Four interrupt sources
- Bus Interface (IIC)
 - Selection of addressing format or non-addressing format
 - Conforms to Philips I2C bus interface (I² C bus format)
 - Two ways of setting slave address (I² C bus format)
 - Start and stop conditions generated automatically in master mode (I² C bus format)
 - Selection of the acknowledge output level in reception (I² C bus format)
 - Automatic loading of an acknowledge bit in transmission (I² C bus format)
 - Wait function in master mode (I² C bus format)
 - Wait function (I² C bus format)
 - Interrupt sources
 - Selection of 16 internal clocks (in master mode)

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- Direct bus drive (SCL/SDA pin)
- Automatic switching from formatless mode to I2C bus format (IIC_0 only)
- Host Interface X-Bus Interface
 - Control of the fast GATE A20 function
 - Shutdown of the XBS module by the HIFSD pin
 - Five host interrupt requests
- Keyboard Buffer Controller
 - Conforms to PS/2 interface specifications
 - Direct bus drive (via the KCLK and KD pins)
 - Interrupt sources: on completion of data reception and on detection of clock edge
 - Error detection: parity error and stop bit monitoring
- Host Interface LPC Interface(LPC)
 - Supports LPC interface I/O read cycles and I/O write cycles
 - Has three register sets comprising data and status registers
 - Supports SERIRQ
 - Eleven interrupt sources
- A/D Converter

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- 10-bit resolution
- Input channels: eight analog input channels and 16 digital input channels
- Analog conversion voltage range can be specified using the reference power supply voltage pin (AVref) as an analog reference voltage
- Conversion time: 13.4 μ s per channel (at 10-MHz operation)
- Two kinds of operating modes
- Four data registers
- Sample and hold function
- Three kinds of conversion start
- Interrupt request
- D/A Converter
 - 8-bit resolution
 - Two output channels
 - Conversion time: Max. 10 μ s (when load capacitance is 20 pF)
 - Output voltage: 0 V to AVref
 - D/A output retaining function in software standby mode
- I/O ports
 - Ten I/O ports (ports 1 to 6, 8, 9, A and B) and one input-only port (port 7)

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- Interrupt Controller
 - Two interrupt control modes
 - Priorities settable with ICR
 - Independent vector addresses
 - Thirty-one external interrupts
 - DTC control
- Power-Down Modes
 - Medium-speed mode
 - Subactive mode
 - Sleep mode
 - Subsleep mode
 - Watch mode
 - Software standby mode
 - Hardware standby mode
 - Module stop mode

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1.3.7 Super I/O – SMSC 10N268

- 3.3 Volt Operation (5 Volt Operation)
- PC99, PC01, ACPI 1.0 Compliant
- LPC Interface Design
- X-Bus Interface (LPC Mode Only)
 - Three Chip Selects (Two I/O and One Memory)
 - 8-Bit Data Transfers
 - Support for Up to 2 MB Flash
 - Interfaces with 3V Memory Devices
 - Support for Up to Two External I/O Components
 - Offers Three Modes of Operation for I/O Devices
 - Provides FWH Emulation
- Serial IRQ Compatible with Serialized IRQ Support for PCI Systems
- Programmable Wake-up Event (PME) Interface
- 33 General Purpose Input/Output Pins
- System Management Interrupt

A790 N/B Maintenance

- 2.88MB Super I/O Floppy Disk Controlle
 - Licensed CMOS 765B Floppy Disk Controller
 - Software and Register Compatible with SMSC's Proprietary 82077AA Compatible Core
 - Supports Two Floppy Drives Directly
 - Configurable Open Drain/Push-Pull Output Drivers
 - Supports Vertical Recording Format
 - 16-Byte Data FIFO
 - 100% IBM Compatibility
 - Detects All Overrun and Under run Conditions
 - Sophisticated Power Control Circuitry (PCC) Including Multiple Power Down Modes for Reduced Power Consumption
 - DMA Enable Logic
 - Data Rate and Drive Control Registers
 - 480 Addresses, Up to 15 IRQ and Four DMA Options

A790 N/B Maintenance

1.3.8 1394B Controller– TI TSB82AA2

- Single 3.3-V supply (1.8-V internal core voltage with regulator)
- 3.3-V and 5-V PCI signaling environments
- Serial bus data rates of 100 M bits/s, 200 M bits/s, 400 M bits/s, and 800 M bits/s
- Physical write posting of up to three outstanding transactions
- Serial ROM or boot ROM interface supports 2-wire serial EEPROM devices
- 33-MHz/64-bit and 33-MHz/32-bit selectable PCI interface
- PCI burst transfers and deep FIFOs to tolerate large host latency
 - Transmit FIFO—5 K asynchronous
 - Transmit FIFO—2 K isochronous
 - Receive FIFO—2 K asynchronous
 - Receive FIFO—2 K isochronous
- D0, D1, D2 and D3 power states and PME events per the PCI Bus Power Management Interface Specification
- Programmable asynchronous transmit threshold

A790 N/B Maintenance

- Isochronous receive dual-buffer mode
- Out-of-order pipelining for asynchronous transmit requests
- Register access fail interrupt when the PHY SYSCLK is not active
- Initial bandwidth available and initial channels available registers
- Digital video and audio performance enhancements
- Fabricated in advanced low-power CMOS process
- Multifunction terminal (MFUNC terminal 1)
 - PCI_CLKRUN protocol per the PCI Mobile Design Guide
 - General-purpose I/O
 - CYCLEIN/CYCLEOUT for external cycle timer control for customized synchronization
- Packaged in 144-terminal LQFP (PGE)

A790 N/B Maintenance

1.3.9 Audio Codec – Realtek ALC260

- Single-chip multi-bit Sigma-Delta converters with high S/N ratio
- 1 stereo DAC supports 16/20/24-bit PCM format with 44.1 K/48 K/96 K/192 kHz sample rate
- 2 stereo ADCs support 16/20-bit PCM format with 44.1K/48K/96kHz sample rate
- Applicable for 2-Channel 192 kHz DVD-Audio solutions
- LINE-OUT, HP-OUT, LINE1, LINE2, MIC1 and MIC2 are stereo input and output re-tasking
- MONO line level output to subwoofer speaker for 2.1 channel applications
- High-quality differential CD analog input
- External PCBEEP input is applicable and internal BEEP generator is integrated
- Power-Off CD mode supported
- Power management and enhanced power saving features
- Power support: Digital: 3.3V; Analog: 3.3V/5.0V
- Selectable 2.5V/3.75V VREFOUT
- Two jack detection pins (each designed to detect 4 jacks)

A790 N/B Maintenance

- Supports 44.1 K/48 K/96 kHz/192 kHz S/PDIF output
- Supports 44.1 K/48 K/96 kHz S/PDIF input
- 48-pin LQFP packages (lead (Pb)-free package also available)
- Supports external volume knob control
- Reserve analog mixer architecture is backwards compatible with AC'97
- -64 dB ~ +30 dB with 1 dB mixer gain for fine volume control
- Impedance sensing capability for each re-tasking jack
- Built-in headphone amplifier for each re-tasking jack
- Supports GPIOs (General Purpose Input/Output) for customized applications
- Hardware copyright protection for DVD-Audio
- Meets Microsoft WHQL/WLP 2.0 audio requirements
- EAX™ 1.0 & 2.0 compatible
- Direct Sound 3D™ compatible
- A3D™ compatible
- I3DL2 compatible

A790 N/B Maintenance

- HRTF 3D Positional Audio
- Emulation of 26 sound environments to enhance gaming experience
- 10-band Software Equalizer
- Voice Cancellation and Key Shifting in Karaoke mode
- Enhanced Configuration Panel and device sensing wizard to improve user experience
- Content Copy Protection for S/PDIF interface
- Power Management setting
- Microphone Acoustic Echo Cancellation (AEC) and Beam Forming (BF) technology for voice application
- Mono/Stereo Microphone Noise Suppression

1.3.10 LAN – Broadcom BCM5752

- Integrates TPM 1.2 security functionality enabling OEMs to offer this high level of PC security as a standard feature
- Enables TPM-ready security platforms for next Microsoft OS (Longhorn)
- Integrates 10/100/1000BASE-T transceiver and media access controller

A790 N/B Maintenance

1.3.11 Mobility VGA chipset – ATI M54CSP128

- The M54/M52 provides the fastest and most advanced 2D, 3D, and multimedia graphics performance for notebooks. The M54/M52 supports Shader Model 3.0, advanced memory interface technology, a brand new display controller and a consumer electronics (CE) quality TV (NTSC/PAL) encoder
- The M54 is based on PCI Express technology and leverages a brand new graphics architecture. Based on 90nm micron process technology, the M54 will deliver a 16-lane PCI Express bus interface and lead-free ASIC

Features in Detail

- 2D Acceleration Features
 - A highly optimized 128-bit engine, capable of processing multiple pixels/clock
 - Hardware acceleration is provided for Bitblt, line drawing, polygon and rectangle fills, bit masking, monochrome expansion, panning and scrolling, scissoring, and full ROP support (including ROP3)
 - Optimized handling of fonts and text using ATI proprietary techniques
 - Game acceleration including support for Microsoft's DirectDraw: Double Buffering, Virtual Sprites, Transparent Blit, and Masked Blit
 - Acceleration in 8/15/16/32 bpp modes
 - Support for WIN 2000 & WIN XP GDI extensions: Alpha BLT, Transparent BLT, Gradient Fill

A790 N/B Maintenance

- Hardware cursor support up to 64x64x32bpp, with alpha channel for direct support of WIN 2000 & WIN XP alpha cursor standard
- 3D Acceleration Features
 - DirectX9 Shader Model 3.0 support
 - Full DX9 conformance, including floating point per component at full speed
 - Support for 2xAA, 4xAA and 6xAA subsamples, with little performance loss in most cases
 - Advanced AA quality algorithms, generating visuals that are superior to other solutions with an equivalent number of samples
 - 2x/4x/8x/16x anisotropic filtering modes. Adaptive algorithm with bi-linear (performance) and tri-linear (quality) options
 - Dedicated geometry acceleration for Direct3D and OpenGL, which incorporates 2 parallel Vector / Scalar Engines performing HW transformation, clipping and lighting
 - 2 full vertex processors in the VAP (Vertex Assembler & Processor)
- Motion Video Acceleration Features
 - Video scaling and fully programmable YCrCb to RGB color space conversion for full-screen / full-speed video playback and fully adjustable color controls
 - Hardware I² C
 - VIP 2.0 with multi channel DMA transfer

A790 N/B Maintenance

- Back end overlay/scaler supports up to 8x4 tap filtering, and always ensures at least 4x2 tap filtering even in extreme cases. 4x4 tap is typical. Back-end scaler also supports upscaling and downscaling, filtered scaling of all supported YUV formats, RGB32 and RGB15/16, and filtered display of images up to 1536 pixels wide
- Provides dramatically reduced CPU utilization without incurring the cost of a full MPEG-2 decoder
- MPEG-4 simple profile support
- Adaptive de-interlacing filter eliminates video artifacts caused by displaying interlaced video on non-interlaced displays, by analyzing image and using optimal de-interlacing function on a per-pixel basis
- Dual Display Features
 - Improved 64-bit display controller with symmetric display capabilities
 - Two triple 10-bit palette DACs (DAC and DAC2) with gamma correction for true WYSIWYG color
Pixel rates up to 400 MHz standard
 - Dual RGB CRT output
 - One C Y COMP output plus second RGB CRT output from second DAC
 - Dual displays (LCD/DVI, DVI/CRT, LCD/TV, CRT/TV, etc.), with completely independent resolution, refresh rates, h/w icon & h/w cursor and display data
 - Hardware cursor up to 64x64 pixels in 2 bpp, full color AND/XOR mix, and full color 8-bit alpha blend
 - Primary display supports VGA and accelerated modes, video overlay, and hardware cursor

A790 N/B Maintenance

- Secondary display supports TV-out or CRT. It supports accelerated modes, video overlay, and hardware cursor; however, it does not support VGA. Modes supported include 800x600 and 16:9 modes such as 848x480, with user flexibility for moving and sizing the screen
- Support for up to 4 k x 4 k resolution display
- Digital Display Support
 - Support for fixed resolution displays (e.g. panels) from VGA (640x480) to wide UXGA (1920x1200) resolution with full ratiometric expansion ability for source modes up to 1400x1050 with standard display timing, or up to 1920x1440 with reduced blanking timing. Higher resolution panels and digital CRTs may be possibly supported - contact ATI for details
 - Improved auto expansion
 - Optional auto-centering mode to display desktop at native size without ratiometric expansion
 - Support for VGA text modes in centering panel modes (up to approximately 165 MHz pixel frequency)
 - Support for reduced blanking intervals, as defined by VESA
- Bus Support Features
 - PCI Express 1.0a and PCI Express 1.1 compliant. PCI Express is the latest generation I/O interconnect architecture which replaces conventional PCI and AGP buses in new PC platforms. Refer to PCI-SIG for specifications relating to PCI Express architecture
 - Native x16 PCI Express bus interface
 - Supports x1, x2, x4, x8, x12, and x16 lane widths

A790 N/B Maintenance

- Supports x16 lane reversal where the receiver on lanes 0 to 15 on the graphics endpoint are mapped to the transmitter on lanes 15 down to 0 on the root complex
- Supports x16 lane reversal where the transmitter on lanes 0 to 15 on the graphics endpoint are mapped the receiver on lanes 15 down to 0 on the root complex (requires corresponding support on the root complex)
- Supports x1, x2, x4, x8, x12 and x16 polarity inversion
- Supports “Mobile Graphics Low-Power Addendum to the PCI Express Base Specification 1.0”
- Memory Support Features
 - 256/128/64-bit memory interface using DDR1 or DDR2 SDRAM/SGRAM, or GDDR3 SDRAM (except M52-T) to build 16/32/64/128/256/512 MB configurations
 - Support for SSTL-1.8 memory interface
- Power Management Features
 - Single chip solution in 90nm micron CMOS technology
 - Full ACPI 1.0b, OnNow, and IAPC (Instantly Available PC) power management
 - Static and dynamic Power Management support (APM as well as ACPI) with full VESA DPM and Energy Star compliance
 - Full POWERPLAY™ 6.0, including enhanced POWER ON DEMAND support
 - The Chip Power Management Support logic supports four device power states - On, Standby, Suspend and Off - defined for the OnNow Architecture. Each power state can be achieved by software control bits

A790 N/B Maintenance

- Clocks to every major functional block are controlled by a unique dynamic clock switching technique which is completely transparent to the software. By turning off the clock to the block that is idle or not used at that point, the power consumption is significantly reduced during normal operation
- Internal LVDS Spread Spectrum Support
 - The M54/M52 Spread Spectrum controller is capable of generating a triangular frequency modulation profile. The amount of spread and the modulation frequency is fully programmable
 - Only the LVDS display is available to be spread (i.e., 1 PLL)
- External Spread Spectrum Support
 - Memory and/or core clock spread spectrum support via the GPIO16 pin
 - External spread spectrum supported for TMDS or LVDS transmitters via the GENERICC/GENERICD pin
- PC Design Guide Compliance
 - Fully compliant with Windows Logo Program requirements for all target Operating Systems. This includes both the current Logo requirements and the future (draft) requirements that will be enforced during the lifespan of the product
 - Fully compliant with Mobile PCI rev 1.0
 - Bi-endian support for compliance on a variety of processor platforms
- Test Capability Features

A790 N/B Maintenance

- Full scan implementation on the digital core logic which provides high fault coverage through ATPG (Automatic Test Pattern Generation Vectors)
- Dedicated test logic for the on-chip custom memory macros to provide complete coverage on these modules
- A JTAG test mode (which is largely compliant with the IEEE 1149.1 standard) including internal scan chain for access to chip-level test functions and for board level connectivity testing
- Integrated hardware diagnostic tests performed automatically upon initialization
- High quality components through built-in Scan and chip diagnostics
- Improved access to the analog modules and PLLs in the M54/M52 in order to allow full evaluation and characterization of these modules
- Other Features
 - Support for serial ROM video BIOS
 - Support for 32 and 64-bit operating systems based on Intel, AMD and PowerPC CPUs
 - HW cursor support for monochrome, color and alpha blended cursors
 - Support for serial ROM video BIOS
 - Support for 32 and 64-bit operating systems based on Intel, AMD and PowerPC CPUs
 - HW cursor support for monochrome, color and alpha blended cursors
 - GDI support for Alpha & Transparent BLTs, as well as Gradient Fills

A790 N/B Maintenance

- Compliance with Wassenaar Agreement
 - 3D vector rate (as defined by the Wassenaar Agreement) is 58 - 78 M 10-pixel vectors/sec

1.3.12 USB Bluetooth (option) – Tecom BT3014

- Bluetooth Specification V.1.2 compliant
- Bluetooth spec 1.1 compatible
- Bluetooth protocol stacks and profiles support is optional
- Indoor coverage range up to 50 m typically in general environments for the Class 1 output power with 0dBi omni-directional antenna
- Outdoor coverage range up to 100 m typically in open site for the Class 1 output power with 0dBi omni-directional antenna
- Output power controllable
- Max data rate 720 kbps

A790 N/B Maintenance

1.3.13 Fax/Modem – ASKEY 1456VQL-T1 (INT-LF)

- HD audio, AC'97, MC'97 2.2 compliant
- V.44, V.42, V.42bis, and MNP TM Class 5 data compression
- Low-power standby mode
- 3.3 V to 5 V power supply
- Compliant with FCC, CTR21, JATE and other PTTs
- Auto sensing host interface to select AC'97 or HD audio
- Operation Temperature/Humidity : 0° C/0%~60° C/90%
- Storage Temperature/Humidity : -20° C/0%~70° C/90%

1.3.14 South Bridge ICH7-M

- PCI Bus Interface
 - Supports PCI Revision 2.3 Specification at 33 MHz
 - Supports up to 6 master devices on PCI
 - NEW: Six available PCI REQ/GNT pairs

A790 N/B Maintenance

- Support for 64-bit addressing on PCI using DAC protocol
- PCI Express Interface
 - 4 PCI Express root ports
 - NEW: 2 Additional PCI Express root ports(Not available on all ICH7 SKUs)
 - Supports PCI Express 1.0a
 - Ports 1-4 can be statically configured as 4x1,or 1x4
 - Support for full 2.5 Gb/s bandwidth in each direction per x1 lane
 - Module based Hot-Plug supported(e.g., ExpressCard)
- Integrated Serial ATA Host Controller
 - two ports (Mobile Only)
 - Integrated AHCI controller(Not available on all ICH7 SKUs)
- Integrated IDE Controller
 - Independent timing of up to two drives
 - Ultra ATA 100/66/33, BMIDE and PIO modes
 - Tri-state modes to enable swap bay
- USB2.0
 - Includes four UHCI host controllers that support eight external port

A790 N/B Maintenance

- Includes one EHCI high-speed USB 2.0 Host Controller that supports all eight ports
- Includes one USB 2.0 High-speed Debug port
- Supports wake-up from sleeping states S1-M-S5
- Supports legacy keyboard/mouse software
- Intel® High Definition Audio Interface
 - PCI Express endpoint
 - Independent Bus Master logic for eight general purpose streams: four input and four output
 - Support three external Codecs
 - Supports variable length stream slots
 - Supports variable length stream slots
 - Provides mic array support
 - Allows for non-48 kHz sampling output
 - Support for ACPI Device States
 - NEW: Docking Support
 - NEW: Low Voltage Mode
- Interrupt Controller
 - Support up to eight PCI interrupt pins
 - Supports PCI 2.3 message signaled interrupts

A790 N/B Maintenance

- Two cascaded 82C59 with 15 interrupts
- Integrated I/O APIC capability with 24 interrupts
- Supports processor system bus interrupt delivery
- 1.05 V operation with 1.5V and 3.3 V I/O
 - 5V tolerant buffers on IDE, PCI, USB over-current and legacy signals
- Timers Based on 82C54
 - System timer, refresh request, speaker tone output
- Power Management Logic
 - ACPI 2.0 compliant
 - ACPI-defined power states (C1–C4, S1–M, S3–S5)
 - ACPI power management timer
 - Support for “Intel® SpeedStep™ technology” processor power control
 - Support for “Deeper Sleep” power state
 - PCI CLKRUN# and PME# support
 - SMI# generation
 - All registers readable/restorable for proper resume from 0 V suspend states
 - Support for APM-based legacy power management for non-ACPI Desktop and Mobile implementation

A790 N/B Maintenance

- External Glue Integration
 - Integrated pull-up, pull-down and series termination resistors on IDE, processor interface
 - Integrated Pull-down and Series resistors on USB
- NEW: Serial Peripheral Interface (SPI) for Serial and Shared Flash
- Firmware Hub (FWH) Interface supports BIOS memory size up to 8 MB
- Low Pin Count (LPC) Interface
 - Supports two Master/DMA devices
 - Support for Security Device (Trusted Platform Module) connected to LPC
- Enhanced DMA Controller
 - Two cascaded 8237 DMA controllers
 - Supports LPC DMA
- Real-Time Clock
 - 256-byte battery-backed CMOS RAM
 - Integrated oscillator components
 - Lower Power DC/DC Converter implementation
- System TCO Reduction Circuits
 - Timers to generate SMI# and Reset upon detection of system hang

A790 N/B Maintenance

- Timers to detect improper processor reset
- Integrated processor frequency strap logic
- Supports ability to disable external devices
- SMBus
 - Flexible SMBus/SMLink architecture to optimize for ASF
 - Provides independent manageability bus through SMLink interface
 - Supports SMBus 2.0 Specification
 - Host interface allows processor to communicate via SMBus
 - Slave interface allows an internal or external microcontroller to access system resources
 - Compatible with most two-wire components that are also I2C compatible
- NEW: 1.05V Core Voltage
- Integrated 1.05V Voltage Regulator (INTVR) for the Suspend and LAN wells
- GPIO
 - TTL, open-drain, inversion
- Package 31x31 mm 652 mBGA

A790 N/B Maintenance

1.3.15 LED Indicators

- There are 7 LED indicators locate on the system Housing, the detail shows on the follows table

LED Number	Functions	LED color	Remark
LED SW BD D19	Power on/Suspend	Green/ Orange	Green : System Power on(Main on =1) Orange : System enter suspend
LED SW BD D20	AC / Charger indicator	Green/ Orange	Green : (System power on & AC exist) or (AC exist & Orange : Battery is charging (No matter System is turning on or off)
LED SW BD D21	Battery Status indicator (AC is not exist)	Green/ Orange	Green : One of Batteries is exist(Reflecting VBat1,VBat2,VBat3) & All of Batteries Cap are over Orange(cont) : One of Bay1,Bay2 Battery Cap is under 5% & Primary is not exist. Orange(flash) : Primary Battery Cap is under 5%(No matter Bay1, Bay2 is exist)
LED SW BD D15	Caps Lock	Yellow	Keyboard Caps Lock
LED SW BD D16	Scroll Lock	Yellow	Keyboard Scroll Lock
LED SW BD D17	Num Lock	Yellow	Keyboard Num Lock
LED SW BD D18	Battery Low	Yellow	If battery in Low state, amber LED blinks.

A790 N/B Maintenance

1.3.16 Buttons

- Power on (SW1) – Push Button for Power on and off control

1.3.17 Mini PCI Interface

- Mechanical dimension support the Mini PCI card Type IIIB
- Mini PCI Interface – Pin out of System Connector

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	TIP	2	RING	63	3.3V	64	FRAME#
	Key		Key	65	CLKRUN#	66	TRDY#
3	8PMJ-33,4	4	8PMJ-13,4	67	SERR#	68	STOP#
5	8PMJ-63,4	6	8PMJ-23,4	69	GROUND	70	3.3V
7	8PMJ-73,4	8	8PMJ-43,4	71	PERR#	72	DEVSEL#
9	8PMJ-83,4	10	8PMJ-53,4	73	C/BE[1]#	74	GROUND
11	LED1_GR NP	12	LED2_YE LP	75	AD[14]	76	AD[15]
13	LED1_GR NN	14	LED2_YE LN	77	GROUND	78	AD[13]
15	CHSGND	16	RESERVE D	79	AD[12]	80	AD[11]
17	INTB#	18	5V	81	AD[10]	82	GROUND
19	3.3V	20	INTA#	83	GROUND	84	AD[09]
21	RESERVE D	22	RESERVE D	85	AD[08]	86	C/BE[0]#
23	GROUND	24	3.3VAUX	87	AD[07]	88	3.3V

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Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
25	CLK	26	RST#	89	3.3V	90	AD[06]
27	GROUND	28	3.3V	91	AD[05]	92	AD[04]
29	REQ#	30	GNT#	93	RESERVE D	94	AD[02]
31	3.3V	32	GROUND	95	AD[03]	96	AD[00]
33	AD[31]	34	PME#	97	5V	98	RESERVE D WIP5
35	AD[29]	36	RESERVE D	99	AD[01]	100	RESERVE D WIP5
37	GROUND	38	AD[30]	101	GROUND	102	GROUND
39	AD[27]	40	3.3V	103	AC_SYNC	104	M66EN
41	AD[25]	42	AD[28]	105	AC_SDAT A IN	106	AC_SDAT A OUT
43	RESERVE D	44	AD[26]	107	AC_BIT_C LK	108	AC_CODE C ID0#
45	C/BE[3]#	46	AD[24]	109	AC_CODE C ID1#	110	AC_RESE T#
47	AD[23]	48	IDSEL	111	MOD_AU DIO MON	112	RESERVE D
49	GROUND	50	GROUND	113	AUDIO_G ND	114	GROUND
51	AD[21]	52	AD[22]	115	SYS_AUD IO_OUT	116	SYS_AUD IO_IN
53	AD[19]	54	AD[20]	117	SYS_AUD IO_OUT GND	118	SYS_AUD IO_IN GND
55	GROUND	56	PAR	119	AUDIO_G ND	120	AUDIO_G ND
57	AD[17]	58	AD[18]	121	RESERVE D	122	MPCIACT #
59	C/BE[2]#	60	AD[16]	123	VCC5VA	124	3.3VAUX
61	IRDY#	62	GROUND				

A790 N/B Maintenance

1.3.18 I/O Ports

1.3.18.1 RJ-11 Modem Line & RJ-45 with LED Connector

<i>Pin</i>	<i>Signal Name</i>	<i>Power On default Direction</i>	<i>S0 State</i>	<i>S3 State</i>	<i>S4 State</i>	<i>Description</i>
1	C_MDI0+	I/O				Transfer differential
2	C_MDI0-	I/O				Receiver differential
3	C_MDI1+	I/O				Transfer differential
4	C_MDI2+	I/O				Transfer differential
5	C_MDI2-	I/O				Receiver differential
6	C_MDI1-	I/O				Receiver differential
7	C_MDI3+	I/O				Transfer differential
8	C_MDI3-	I/O				Receiver differential
9	LINKLED	O				LINKLED
10	LED_PWR	Power				LED_PWR
11	TRAFFICLED#	O				TRAFFICLED#
12	SPD100/1000LED#	O				SPD100/1000LED#
13	LED_PWR	Power				LED_PWR
A1	MODEMN	I/O				MODEMN
A2	MODEMP	I/O				MODEMP

A790 N/B Maintenance

1.3.18.2 Infrared interface supporting IRDA format (HSD3602)

- Fully Compliant to IrDA 1.1 Physical Layer Specifications (9.6 Kb/s to 4 Mb/s operation)
- Typical Link Distance of = 1.0 m
- Low Power Operation of 3.3 V
- Small Module Size of Height 4.0 mm, Width 12.2 mm, Depth 5.1 mm
- Complete Shutdown (TXD, RXD, PIN Diode)
- Low Shutdown Current of 10 nA typical
- Single Rx Data Output allowing speed select by FIR select pin
- Excellent noise immunity with Integrated EMI Shield
- Edge Detection Input feature preventing the LED from long turn-on time
- Interface to Various Super I/O and Controller Devices
- Designed to accommodate light loss with Cosmetic Window

A790 N/B Maintenance

Pin	Signal Name	Power On default Direction	S0 State	S3 State	S4 State	Description
1	VCC	Power off	+3V	Chip Power off	Power off	Supply Voltage
2	AGND	Ground	Ground	Ground	Ground	Analog Ground
3	FIR_SEL	In	Out	Chip Power off	Power off	FIR Select
4	AGND	Ground	Ground	Ground	Ground	Analog Ground
5	MD0	In	Out	Chip Power off	Power off	Mode 0
6	MD1	In	Out	Chip Power off	Power off	Mode 1
7	NC	-	-	-	-	No Connection
8	GND	Ground	Ground	Ground	Ground	Ground
9	RXD	In	In	Chip Power off	Power off	Receiver Data Output
10	TXD	Out	Out	Chip Power off	Power off	Transmitter Data Input

A790 N/B Maintenance

1.3.18.3 USB Ports – SUYIN 020151MR008S511ZU

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Description
A1	USB1_5V	0V	5V	5V	5V	Supply voltage
A2	USB1-	Low	I/O	Low	Low	USB Differential Data Minus
A3	USB1+	Low	I/O	Low	Low	USB Differential Data Plus
A4	GND	Ground	Ground	Ground	Ground	Ground
B1	USB2_5V	0V	5V	5V	5V	Supply voltage
B2	USB2-	Low	I/O	Low	Low	Data -
B3	USB2+	Low	I/O	Low	Low	Data +
B4	GND	Ground	Ground	Ground	Ground	Ground
GND1	GND	Ground	Ground	Ground	Ground	Shield
GND2	GND	Ground	Ground	Ground	Ground	Shield
GND3	GND	Ground	Ground	Ground	Ground	Shield
GND4	GND	Ground	Ground	Ground	Ground	Shield
GND5	GND	Ground	Ground	Ground	Ground	Shield
GND6	GND	Ground	Ground	Ground	Ground	Shield

A790 N/B Maintenance

1.3.18.4 Port Replicator Connector – I-PEX 30029-080T-01-(1)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Description
1	P_GND	P_Ground	P_Ground	P_Ground	P_Ground	P_Ground
2	P_GND	P_Ground	P_Ground	P_Ground	P_Ground	P_Ground
3	DCP1	19V	19V	19V	19V	19V
4	DCP1	19V	19V	19V	19V	19V
5	P_GND	P_Ground	P_Ground	P_Ground	P_Ground	P_Ground
6	P_GND	P_Ground	P_Ground	P_Ground	P_Ground	P_Ground
7	DCP1	19V	19V	19V	19V	19V
8	DCP1	19V	19V	19V	19V	19V
9	P_GND	P_Ground	P_Ground	P_Ground	P_Ground	P_Ground
10	P_GND	P_Ground	P_Ground	P_Ground	P_Ground	P_Ground
11	DCP1	19V	19V	19V	19V	19V
12	DCP1	19V	19V	19V	19V	19V
13	P_GND	P_Ground	P_Ground	P_Ground	P_Ground	P_Ground
14	P_GND	P_Ground	P_Ground	P_Ground	P_Ground	P_Ground
15	DCP1	19V	19V	19V	19V	19V
16	DCP1	19V	19V	19V	19V	19V
17	PIO_PD0		I/O			PIO Data bit0 signal
18	PIO_STROBE		O			PIO Strobe
19	+5VS	+5VS	+5VS	0	0	+5V
20	PIO_PD1		I/O			PIO Data bit1 signal

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1.3.18.4 Port Replicator Connector – I-PEX 30029-080T-01-(2)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Description
21	PIO_PD2		I/O			PIO Data bit2 signal
22	PIO_PE		I			PIO Printer Paper End
23	+5VS	+5V	+5V	0	0	+5V
24	PIO_PD3		I/O			PIO Data bit3 signal
25	PIO_PD4		I/O			PIO Data bit4 signal
26	PIO_ERROR		I			PIO Printer Error
27	+3VS	+3VS	+3VS	0	0	+3VS
28	PIO_PD5		I/O			PIO Data bit5 signal
29	PIO_PD6		I/O			PIO Data bit6 signal
30	PIO_ALF		O			PIO Auto Feed
31	+3VS	+3VS	+3VS	0	0	+3VS
32	PIO_PD7		I/O			PIO Data bit7 signal
33	PIO_SLCTI N		I			PIO printer Select Input
34	PIO_INIT		O			PIO Printer Initiate
35	+5V	+5V	+5V	+5V	0	+5V
36	PIO_SLCT		I			PIO Printer Selected Status
37	P_GND	P_Ground	P_Ground	P_Ground	P_Ground	P_Ground
38	PIO_BUSY		I			PIO Printer Busy
39	P_GND	P_Ground	P_Ground	P_Ground	P_Ground	P_Ground
40	PIO_ACK		I			PIO Printer Acknowledge

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1.3.18.4 Port Replicator Connector – I-PEX 30029-080T-01-(3)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Description
41	USBP3+		I/O			USB Differential Data Plus
42	D/RI#		IN			COM1 Ring indicator signal
43	USBP3-		I/O			USB Differential Data Minus
44	USBOC3#		I			USB over current to USB HUB
45	P_GND	P_Ground	P_Ground	P_Ground	P_Ground	P_Ground
46	D/DCD#		IN			COM1 Carrier detector signal
47	P_GND	P_Ground	P_Ground	P_Ground	P_Ground	P_Ground
48	D/DSR#		IN			COM1 Data set ready signal
49	P_GND	P_Ground	P_Ground	P_Ground	P_Ground	P_Ground
50	D/RXD		IN			COM1 Received data signal
51	DK_RED		O			RED for docking CRT
52	DK_HSYNC		O			Hsync for docking CRT
53	P_GND	P_Ground	P_Ground	P_Ground	P_Ground	P_Ground
54	D/RTS#		O			COM1 Request to send signal
55	DK_GREEN		O			GREEN for docking CRT
56	DK_VSYNC		O			Vsync for docking CRT
57	P_GND	P_Ground	P_Ground	P_Ground	P_Ground	P_Ground
58	D/TXD		O			COM1 Transmitted data signal
59	DK_BLUE		O			BLUE for docking CRT
60	DK_DDCLK		I/O			EDIT For docking CRT

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1.3.18.4 Port Replicator Connector – I-PEX 30029-080T-01-(4)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Description
61	P_GND	P_Ground	P_Ground	P_Ground	P_Ground	P_Ground
62	D/CTS#		IN			COM1 Clear to send signal
63	P_GND	P_Ground	P_Ground	P_Ground	P_Ground	P_Ground
64	DK_DDDAT A		I/O			EDIT For docking CRT
65	P_GND	P_Ground	P_Ground	P_Ground	P_Ground	P_Ground
66	D/DTR#		O			COM1 Data terminal ready signal
67	D/DCD#4		IN			COM4 Carrier detector signal
68	D/RXD		IN			COM4 Received data signal
69	D/TXD		O			COM4 Transmitted data signal
70	D/DTR#4		O			COM4 Data terminal ready signal
71	D/DSR#4		IN			COM4 Data set ready signal
72	D/RTS#4		O			COM4 Request to send signal
73	D/CTS#4		IN			COM4 Clear to send signal
74	D/RI#4		IN			COM4 Ring indicator signal
75	P_GND	P_Ground	P_Ground	P_Ground	P_Ground	P_Ground
76	P_GND	P_Ground	P_Ground	P_Ground	P_Ground	P_Ground
77	IGN		I			Ignition input
78	PIO/PNF#		I			Parallel port
79	+3V	+3V	+3V	+3V		+3V
80	PORTREP_EN		o			Indicate Replicator status

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1.3.18.5 Micphone Connector- SMKLGY3319

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
1	CAGND	Power			-	Audio GND
2	CAGND	Power			-	Audio GND
3	MIC1_IN_R	I			Input	Microphone Input Right Signal
4	MIC1_IN_L	I			Input	Microphone Input Left Signal
5	CAGND	Power			-	Audio GND

1.3.18.6 Stereo Jack Connector SMKLGY3319

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
1	DEVICE_DECT#	I				Audio and Optical Fiber Device detect
2	CAGND	Power			-	Audio GND
3	Line out right	I				Audio Line out right signal
4	Line out left	I				Audio Line out left signal
5	CAGND	Power				Audio GND

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1.3.18.7 Parallel Port Connector –(Mitac 331040009005)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
1	P_STB#	O				PIO Strobe
2	P_LPD0	I/O				PIO Data bit0 signal
3	P_LPD1	I/O				PIO Data bit1 signal
4	P_LPD2	I/O				PIO Data bit2 signal
5	P_LPD3	I/O				PIO Data bit3 signal
6	P_LPD4	I/O				PIO Data bit4 signal
7	P_LPD5	I/O				PIO Data bit5 signal
8	P_LPD6	I/O				PIO Data bit6 signal
9	P_LPD7	I/O				PIO Data bit7 signal
10	PIO_ACK#	I				PIO Printer Acknowledge
11	D/BUSY	I				PIO Printer Busy
12	D/PE	I				PIO Printer Paper End
13	D/SLCT	I				PIO Printer Selected Status
14	D/AFD#	O				PIO Auto Feed
15	PIO/ERROR#	I				PIO Printer Error
16	PIO/INIT#	O				PIO Printer Initiate
17	D/SLIN#	I				PIO printer Select Input
18,19,20,21,22,23,24,25	PIO-GND	Ground				Ground

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1.3.18.8 VGA Port Connector–(Mitac 331040009005)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
1	CRT1_RED	O				CRT RED SIGNAL
2	CRT1_GREEN	O				CRT GREEN SIGNAL
3	CRT1_BLUE	O				CRT BLUE SIGNAL
4	GND	Power				GND
5	Ground	Power				GND
6	Ground	Power				GND
7	Ground	Power				GND
8	Ground	Power				GND
9	+5VS	Power				+5VS
10	Ground	Power				Ground
11	NC	-				No Connect
12	CRT1_DD CDATA	I				DDC Data Signal
13	CRT1_HSYNC	O				CRT Horizontal Sync. Signal
14	CRT1_VSYNC	O				CRT Vertical Sync. Signal
15	CRT1_DD CCLK	I				DDC Data Signal

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1.3.18.9 Serial 9 Pin Male Connector

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose	Voltage level
1	D/DCD#	I				Serial –COM1	+/-7.25V
2	D/RXD	I				Serial –COM1	+/-7.25V
3	D/TXD	O				Serial –COM1	+/-7.25V
4	D/DTR#	O				Serial –COM1	+/-7.25V
5	GND	-				Ground	-
6	D/DSR#	I				Serial –COM1	+/-7.25V
7	D/RTS#	O				Serial –COM1	+/-7.25V
8	D/CTS#	I				Serial –COM1	+/-7.25V
9	D/RI#	I				Serial –COM1	+/-7.25V

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1.3.19 Internal Connector Definition

1.3.19.1 LCD Connector 40 Pin- LVC-C40SFYG-(1)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
1	LCD_ID0	I				LCD ID0
2	LCD_ID1	I				LCD ID1
3	LCD_ID2	I				LCD ID2
4	TP1	-				TEST POINT
5	TP2	-				TEST POINT
6	+5VS	+5VS	+5VS	0	0	+5VS
7	DDCPCLK	I				EDID CLK input
8	DDCPDATA	I				EDID DATA input
9	GND	Power				Ground
10	TXOUT10-	O				Transmission Data of Pixels 0(Negative : -)
11	TXOUT10+	O				Transmission Data of Pixels 0(Positive : +)
12	GND	Power				Ground
13	TXOUTCLK1-	O				Sampling Clock(Negative : -)
14	TXOUTCLK1+	O				Sampling Clock(Positive : +)
15	GND	Power				Ground
16	TXOUT12-	O				Transmission Data of Pixels 2(Negative : -)
17	TXOUT12+	O				Transmission Data of Pixels 2(Negative : +)
18	GND	Power				Ground

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1.3.19.1 LCD Connector 40 Pin- LVC-C40SFYG-(2)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
19	TXOUT11-	O				Transmission Data of Pixels 1(Negative : -)
20	TXOUT11+	O				Transmission Data of Pixels 1(Negative : +)
21	GND	Power				Ground
22	GND	Power				Ground
23	GND	Power				Ground
24	GND	Power				Ground
25	TXOUT20-	O				Transmission Data of Pixels 0(Negative : -)
26	TXOUT20+	O				Transmission Data of Pixels 0(Positive : +)
27	GND	Power				Ground
28	TXOUTCLK2-	O				Sampling Clock(Negative : -)
29	TXOUTCLK2+	O				Sampling Clock(Positive : +)
30	GND	Power				Ground
31	TXOUT22-	O				Transmission Data of Pixels 2(Negative : -)
32	TXOUT22+	O				Transmission Data of Pixels 2(Negative : +)
33	GND	Power				Ground
34	TXOUT21-	O				Transmission Data of Pixels 1(Negative : -)
35	TXOUT21+	O				Transmission Data of Pixels 1(Negative : +)

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1.3.19.1 LCD Connector 40 Pin- LVC-C40SFYG-(3)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
36	GND	Power				Ground
37	LCDVCC	O				+3V with fuse controlled by EN VDD video controller
38	LCDVCC	O				+3V with fuse controlled by EN VDD video controller
39	LCDVCC	O				3V with fuse controlled by EN VDD video controller
40	LCDVCC	O				3V with fuse controlled by EN VDD video controller

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1.3.19.2 KBD Connector 40 Pin- ELCO6229-(1)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
1	TPD_DATA	I				Touch Pad DATA
2	TPD_CLK	I				Touch Pad CLOCK
3	KBD_KO15	O				KBD matrix
4	KBD_KO14	O				KBD matrix
5	KBD_KO13	O				KBD matrix
6	KBD_KO12	O				KBD matrix
7	KBD_KO11	O				KBD matrix
8	KBD_KO10	O				KBD matrix
9	KBD_KO9	O				KBD matrix
10	KBD_KO8	O				KBD matrix
11	KBD_KO7	O				KBD matrix
12	KBD_KO6	O				KBD matrix
13	KBD_KO5	O				KBD matrix
14	KBD_KO4	O				KBD matrix
15	KBD_KO3	O				KBD matrix
16	KBD_KO2	O				KBD matrix
17	KBD_KO1	O				KBD matrix
18	KBD_KO0	O				KBD matrix
19	KBD_EN_EL	I				Key board back light EN/EL
20	KBD_US/JP#	I				Indicator US/JP Key board

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1.3.19.2 KBD Connector 40 Pin- ELCO6229-(2)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
21	KI7	I				KBD matrix
22	KI3	I				KBD matrix
23	KI6	I				KBD matrix
24	KI2	I				KBD matrix
25	KI5	I				KBD matrix
26	KI1	I				KBD matrix
27	KI4	I				KBD matrix
28	KI0	I				KBD matrix
29	KBD_GND	Power				GND
30	KBD_GND	Power				GND
31	KBD_GND	Power				GND
32	KBD_GND	Power				GND
33	KBD_GND	Power				GND
34	KBD_GND	Power				GND
35	+12VS	Power				Key board back light Power
36	+5V	Power				Touch pad Power
37	+12VS	Power				Key board back light Power
38	+5V	Power				Touch pad Power
39	+12VS	Power				Key board back light Power
40	+5V	Power				Touch pad Power

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1.3.19.3 RTC Battery Connector 2 Pin- Hirose DF13-2P

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
1	+3VA	+3VA	+3VA	+3VA	+3VA	+3VA
2	GND	Power				GND

- The charge function will not support for RTC battery
- The consumption of RTC CMOS memory will be ~3uA, the calculated life cycle for the RTC battery is no less than 3 years

1.3.18.4 PCMCIA Connector 68 Pin- FCI 62601-22L0C (Mitac 344600030001)-(1)

Pin No	Pin Name	Power On default Direction	S0 State	S3 State	S4 State	Description
2	CAD0	I/O				Card Bus address/data bus
3	CAD1	I/O				Card Bus address/data bus
37	CAD2	I/O				Card Bus address/data bus
4	CAD3	I/O				Card Bus address/data bus
38	CAD4	I/O				Card Bus address/data bus
5	CAD5	I/O				Card Bus address/data bus

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1.3.19.4 PCMCIA Connector 68 Pin- FCI 62601-22L0C (Mitac 344600030001)-(2)

Pin No	Pin Name	Power On default Direction	S0 State	S3 State	S4 State	Description
39	CAD6	I/O				Card Bus address/data bus
6	CAD7	I/O				Card Bus address/data bus
41	CAD8	I/O				Card Bus address/data bus
8	CAD9	I/O				Card Bus address/data bus
42	CAD10	I/O				Card Bus address/data bus
9	CAD11	I/O				Card Bus address/data bus
10	CAD12	I/O				Card Bus address/data bus
44	CAD13	I/O				Card Bus address/data bus
11	CAD14	I/O				Card Bus address/data bus
45	CAD15	I/O				Card Bus address/data bus
46	CAD16	I/O				Card Bus address/data bus
55	CAD17	I/O				Card Bus address/data bus
22	CAD18	I/O				Card Bus address/data bus
56	CAD19	I/O				Card Bus address/data bus
23	CAD20	I/O				Card Bus address/data bus
24	CAD21	I/O				Card Bus address/data bus
25	CAD22	I/O				Card Bus address/data bus
26	CAD23	I/O				Card Bus address/data bus
27	CAD24	I/O				Card Bus address/data bus
28	CAD25	I/O				Card Bus address/data bus
29	CAD26	I/O				Card Bus address/data bus
30	CAD27	I/O				Card Bus address/data bus

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1.3.19.4 PCMCIA Connector 68 Pin- FCI 62601-22L0C (Mitac 344600030001)-(3)

Pin No	Pin Name	Power On default Direction	S0 State	S3 State	S4 State	Description
64	CAD28	I/O				Card Bus address/data bus
31	CAD29	I/O				Card Bus address/data bus
65	CAD30	I/O				Card Bus address/data bus
66	CAD31	I/O				Card Bus address/data bus
7	CC/BE0#	I/O				Card Bus bus commands and byte enables.
12	CC/BE1#	I/O				Card Bus bus commands and byte enables.
21	CC/BE2#	I/O				Card Bus bus commands and byte enables.
61	CC/BE3#	I/O				Card Bus bus commands and byte enables.
13	CPAR	I/O				Card Bus bus parity
14	CPERR#	I/O				Card Bus parity error indicator
15	CGNT#	O				Card Bus bus grant
16	CINT#	I				Card Bus interrupt
20	CIRDY#	I/O				Card Bus initiator ready
33	CCLKRUN#	I				Card Bus clock run
36	CCD1#	I				Card Bus detect 1
43,57	CVS1,CVS2	Power				Cars Bus voltage sense 1 and Card Bus detect 2
48	CBLOCK#	I/O				Card Bus lock
49	CSTOP#	I/O				Cars Bus stop
50	CDEVSEL#	I/O				Card Bus device select

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1.3.19.4 PCMCIA Connector 68 Pin- FCI 62601-22L0C (Mitac 344600030001)-(4)

Pin No	Pin Name	Power On default Direction	S0 State	S3 State	S4 State	Description
53	CTRDY#	I/O				Card Bus target ready
54	CFRAME#	I/O				Card Bus cycle frame
58	CRST#	O				Card Bus reset
59	CSERR#	I				Card Bus system error
60	CREQ#	I				Card Bus request
62	CAUDIO	O				Card Bus audio
63	CSTSCHG	I				Card Bus states change
67	CCD2#	I				Card Bus detect 1
19	CCLK	I				Card Bus clock
17,51	CARD_VCC	Power				Switched output that delivers 0 V, 3.3-V, 5-V, or high impedance to card
18,52	VPPOUT	Power				Switched output that delivers 0 V 3.3-V, 5-V, 12-V, or high impedance to card

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1.3.19.5 Mini PCI-Express-(1)

- Mechanical dimension support the Mini Card.
- Mini PCI_E Interface – Pin out of System Connector

Pin	Signal	Pin	Signal
1	PCIE_WAKE#	2	3.3VS
3	WLAN_AACTIVE	4	GROUND
5	BT_ACTIVE	6	1.5VS
7	PCIECLKREQ	8	NC
9	GROUND	10	NC
11	CLK_PCIE_S1	12	NC
13	CLK_PCIE_S1	14	NC
15	GROUND	16	NC
17	TP	18	GROUND
19	TP	20	MINI_PD#
21	GROUND	22	BUF_PLT_RST#
23	PCIE_RXN3	24	3.3V
25	PCIE_RXP3	26	GROUND
27	GROUND	28	1.5VS
29	GROUND	30	SMBCLK
31	PCIE_TXN3	32	SMBDATA
33	PCIE_TXP3	34	GROUND
35	GROUND	36	NC
37	NC	38	NC

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1.3.19.5 Mini PCI-Express-(2)

Pin	Signal	Pin	Signal
39	NC	40	GROUND
41	NC	42	S1_LED0
43	NC	44	S1_LED1
45	NC	46	S1_LED2
47	NC	48	1.5VS
49	NC	50	GROUND
51	NC	52	3.3V
53	GROUND	54	GROUND

1.3.19.6 IDE 52 Pin Connector-(1)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
1	GND	Power				Ground
2	GND	Power				Ground
3	GND	Power				Ground
4	GND	Power				Ground
5	IDE_HDD_THRM-	O				HDD Thermal sensor Negative
6	IDE_HDD_THRM+	O				HDD Thermal sensor Positive

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1.3.19.6 IDE 52 Pin Connector-(2)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
7	TEMP_SEN	O				Temperature sensor
8	+5VA	Power				Temperature sensor Power
9	+5VS_HDD	Power				HDD POWER
10	GND	Power				GND
11	GND	Power				GND
12	+5VS_HDD	Power				HDD POWER
13	GND	Power				GND
14	IDE_ENOVA_PCS #3	O				Chip Select signal
15	IDE_HDD_LED#	O				Indicator HDD status
16	IDE_ENOVA_PCS #1	O				Chip Select signal
17	IDE_ENOVA_PAD 2	O				Address 2
18	NC	-				NC
19	IDE_ENOVA_PAD 0	O				Address 0
20	IDE_ENOVA_PAD 1	O				Address 1
21	NC	-				NC
22	GND	Power				GND
23	IDE_ENOVA_IRQ14	O				Interrupt signal
24	IDE_ENOVA_PDD ACK#	O				DMA Acknowledge

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1.3.19.6 IDE 52 Pin Connector-(3)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
25	GND	Power				GND
26	GND	Power				GND
27	IDE_ENOVA_PIORDY	O				I/O Ready
28	IDE_ENOVA_PDIO#	O				Read Strobe
29	GND	Power				GND
30	GND	Power				GND
31	IDE_ENOVA_PDIOW	O				Write Strobe
32	IDE_ENOVA_PDDREQ	I				DMA Request
33	NC	Power				NC
34	IDE_ENOVA_SD 15	I/O				IDE Device data 15
35	GND	Power				GND
36	IDE_ENOVA_SD 0	I/O				IDE Device data 0
37	IDE_ENOVA_SD 14	I/O				IDE Device data 14
38	IDE_ENOVA_SD 13	I/O				IDE Device data 13

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1.3.19.6 IDE 52 Pin Connector-(4)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
40	IDE_ENOVA_SD 2	I/O				IDE Device data 2
41	IDE_ENOVA_SD 12	I/O				IDE Device data 12
42	IDE_ENOVA_SD 11	I/O				IDE Device data 11
43	IDE_ENOVA_SD 3	I/O				IDE Device data 3
44	IDE_ENOVA_SD 4	I/O				IDE Device data 4
45	IDE_ENOVA_SD 10	I/O				IDE Device data 10
46	IDE_ENOVA_SD 9	I/O				IDE Device data 9
47	IDE_ENOVA_SD 5	I/O				IDE Device data 5
48	IDE_ENOVA_SD 6	I/O				IDE Device data 6
49	IDE_ENOVA_SD 8	I/O				IDE Device data 8
50	GND	Power				GND
51	IDE_ENOVA_SD 7	I/O				IDE Device data 7
52	IDE_ENOVA_RST #	O				Reset

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1.3.19.7 SATA HDD Connector (Mitac 291000025204)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
1月4日	+19V_HEAT	O				Heater Power
5	HDD_D-	O				Remote Thermal Negative Input
6	HDD_D+	O				Remote Thermal Positive Input
7	TEMP_SEN	I				Temperature Sense
8	+5VA	O				Power Supply
9,10,12	+5VS	O				Power Supply
25	SATAHDD_TXN	O				SATA Differential Signal
26	SATAHDD_TXP	O				SATA Differential Signal
29	SATAHDD_RXN	I				SATA Differential Signal
30	SATAHDD_RXP	I				SATA Differential Signal
11,13,18 ,34-52	GND	GND				Ground
14- 17,19- 24,27,28	NC	-				

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1.3.19.8 Speaker Left 2 Pin Connector- HIROSE

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
1	SPKLOUT+	O	2W /4 ohm			Line out to speaker left
2	SPKLOUT-	O	2W /4 ohm			Line out to speaker Left

1.3.19.9 Finger Printer Board 6 Pin Hirose DF13-6P

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
1	+3.3V	Power				+5V POWER
2	USB +	I/O				USB Differential Data Plus
3	USB -	I/O				USB Differential Data
4	GND	Power				Ground
5	GND	Power				Ground
6	GND	Power				Ground

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1.3.19.10 Mother Board to I/O Board (120Pin) Panasonic 1 of 3 J5-(1)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
1,3,11,19,27,35,43,51,59,67,75,91,101,107,113,119,128,16,24,32,40,48,56,64,72,84,90,96,102,108,114,120	GND	Power				Ground
2	PCI_AD0	I/O				AD[31:0] is a multiplexed address and data bus.
4	PCI_AD2	I/O				AD[31:0] is a multiplexed address and data bus.
5	PCI_AD1	I/O				AD[31:0] is a multiplexed address and data bus.
6	PCI_AD4	I/O				AD[31:0] is a multiplexed address and data bus.
7	PCI_AD3	I/O				AD[31:0] is a multiplexed address and data bus.
9	PCI_AD5	I/O				AD[31:0] is a multiplexed address and data bus.
10	PCI_AD6	I/O				AD[31:0] is a multiplexed address and data bus.
12	PCI_AD8	I/O				AD[31:0] is a multiplexed address and data bus.
13	PCI_AD7	I/O				AD[31:0] is a multiplexed address and data bus.

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1.3.19.10 Mother Board to I/O Board (120Pin) Panasonic 1 of 3 J5-(2)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
14	PCI_AD10	I/O				AD[31:0] is a multiplexed address and data bus.
15	PCI_AD9	I/O				AD[31:0] is a multiplexed address and data bus.
17	PCI_AD11	I/O				AD[31:0] is a multiplexed address and data bus.
18	PCI_AD12	I/O				AD[31:0] is a multiplexed address and data bus.
20	PCI_AD14	I/O				AD[31:0] is a multiplexed address and data bus.
21	PCI_AD13	I/O				AD[31:0] is a multiplexed address and data bus.
22	PCI_AD16	I/O				AD[31:0] is a multiplexed address and data bus.
23	PCI_AD15	I/O				AD[31:0] is a multiplexed address and data bus.
25	PCI_AD17	I/O				AD[31:0] is a multiplexed address and data bus.
26	PCI_AD18	I/O				AD[31:0] is a multiplexed address and data bus.
28	PCI_AD20	I/O				AD[31:0] is a multiplexed address and data bus.
29	PCI_AD19	I/O				AD[31:0] is a multiplexed address and data bus.
30	PCI_AD22	I/O				AD[31:0] is a multiplexed address and data bus.
31	PCI_AD21	I/O				AD[31:0] is a multiplexed address and data bus.
33	PCI_AD23	I/O				AD[31:0] is a multiplexed address and data bus.

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1.3.19.10 Mother Board to I/O Board (120Pin) Panasonic 1 of 3 J5-(3)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
34	PCI_AD24	I/O				AD[31:0] is a multiplexed address and data bus.
36	PCI_AD26	I/O				AD[31:0] is a multiplexed address and data bus.
37	PCI_AD25	I/O				AD[31:0] is a multiplexed address and data bus.
38	PCI_AD28	I/O				AD[31:0] is a multiplexed address and data bus.
39	PCI_AD27	I/O				AD[31:0] is a multiplexed address and data bus.
41	PCI_AD29	I/O				AD[31:0] is a multiplexed address and data bus.
42	PCI_AD30	I/O				AD[31:0] is a multiplexed address and data bus.
44	PCI_GNT#0	O				PCI Grants.
45	PCI_AD31	I/O				AD[31:0] is a multiplexed address and data bus.
46	PCI_GNT#1	O				PCI Grants.
47	PCI_REQ#0	I				PCI Requests.
49	PCI_REQ#1	I				PCI Requests.
50	PCI_GNT#2	O				PCI Grants.
52	PCI_GNT#3	O				PCI Grants.
53	PCI_REQ#2	I				PCI Requests.
54	PCI_GNT#4	O				PCI Grants.
55	PCI_REQ#3	I				PCI Requests.

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1.3.19.10 Mother Board to I/O Board (120Pin) Panasonic 1 of 3 J5-(4)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
57	PCI_REQ#4	I				PCI Requests.
58	PCI_GNT#5	O				PCI Grants.
60	PCI_LOCK#	I/O				PCI Lock.
61	PCI_REQ#5	I				PCI Requests.
62	PCI_DEVSEL#	I/O				Device Select.
63	PCI_SERR#	I/OD				System Error.
65	PCI_STOP#	I/O				PCI Stop.
66	PCI_IREDY#	I/O				initiator Ready.
68	PCI_PAR	I/O				Calculated/Checked Parity.
69	PCI_TRDY#	I/O				Target Ready.
70	PCI_PERR#	I/O				Parity Error.
71	PCI_CLKRUN#	I				PCI Clock run.
73	PCI_RST#	O				PCI Reset.
74	PCI_FRAME#	I/O				Cycle Frame.
76	PCI_CBE#0	I/O				Bus Command and Byte Enables.
77	PCI_INTA#	O				Lnitialization.
78	PCI_CBE#1	I/O				Bus Command and Byte Enables.
79	PCI_INTB#	O				Lnitialization.
80	PCI_CBE#2	I/O				Bus Command and Byte Enables.
81	PCI_INTC#	O				Lnitialization.

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1.3.19.10 Mother Board to I/O Board (120Pin) Panasonic 1 of 3 J5-(4)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
82	PCI_CBE#3	I/O				Bus Command and Byte Enables.
83	PCI_INTD#	O				Initialization.
85	PCI_INTE#	O				Initialization.
86,88,103,105	N/A	-				N/A
87	PCI_INTF#	O				Initialization.
89	BAY2_GPIO	I/O				General Purpose I/O Signals
92	USBP0+	I/O				Universal Serial Bus Port0 Differential.
93	USBOC0#	I				Overcurrent Indicators.
94	USBP0-	I/O				Universal Serial Bus Port0 Differential.
95	USBOC1#	I				Overcurrent Indicators.
97	USBOC2#	I				Overcurrent Indicators.
98	USBP1+	I/O				Universal Serial Bus Port1 Differential.
99	USBOC3#	I				Overcurrent Indicators.
100	USBP1-	I/O				Universal Serial Bus Port1 Differential.
104	USBP2+	I/O				Universal Serial Bus Port2 Differential.
106	USBP2-	I/O				Universal Serial Bus Port2 Differential.
109	USBP7-	I/O				Universal Serial Bus Port7 Differential.

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1.3.19.10 Mother Board to I/O Board (120Pin) Panasonic 1 of 3 J5-(5)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
110	USBP3+	I/O				Universal Serial Bus Port3 Differential.
111	USBP7+	I/O				Universal Serial Bus Port7 Differential.
112	USBP3-	I/O				Universal Serial Bus Port3 Differential.
115	USBP5-	I/O				Universal Serial Bus Port5 Differential.
116	USBP4+	I/O				Universal Serial Bus Port4 Differential.
117	USBP5+	I/O				Universal Serial Bus Port4 Differential.
118	USBP4-	I/O				Universal Serial Bus Port4 Differential.

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1.3.19.11 Mother Board to I/O Board (120Pin) Panasonic 2 of 3 J7-(1)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
1,3,5,7,11,15,19,23,33,53,89,93,97,101,105,54,58.	GND	Power				Ground.
2	KBD_KO0	I				Keyboard Matrix coordinate axis Y0. a
4	KBD_KO1	I				Keyboard Matrix coordinate axis Y1. a
6	KBD_KO2	I				Keyboard Matrix coordinate axis Y2. a
8	KBD_KO3	I				Keyboard Matrix coordinate axis Y3. a
9	POWERSW#	Power				Power switch signal.
10	KBD_KO4	I				Keyboard Matrix coordinate axis Y4. a
12	KBD_KO5	I				Keyboard Matrix coordinate axis Y5. a
13	VOL_ADJ	I				Variable Voltage.
14	KBD_KO6	I				Keyboard Matrix coordinate axis Y6. a
16	KBD_KO7	I				Keyboard Matrix coordinate axis Y7. a
17	BLADJ	I				back to the light.
18	KBD_KO8	I				Keyboard Matrix coordinate axis Y8. a
20	KBD_KO9	I				Keyboard Matrix coordinate axis Y9. a

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1.3.19.11 Mother Board to I/O Board (120Pin) Panasonic 2 of 3 J7-(2)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
21	CLK_14.318MHZ	I				Oscillator 14.318MHZ.
22	KBD_KO10	I				Keyboard Matrix a coordinate axis Y10.
24	KBD_KO11	I				Keyboard Matrix a coordinate axis Y11.
25,27	TEST POINT	-				This pin is test point.
26	KBD_KO12	I				Keyboard Matrix a coordinate axis Y12.
28	KBD_KO13	I				Keyboard Matrix a coordinate axis Y13.
29	ADEN#					Adapter in detect
30	KBD_KO14	I				Keyboard Matrix a coordinate axis Y14.
31	USB_CLT	I				Control USB current signal.
32	KBD_KO15	I				Keyboard Matrix a coordinate axis Y15.
34	KBD_KI0	I				Keyboard Matrix a coordinate axis X 0.
35	TPD_DATA	I/O				Touch pad data signal.
36	KBD_KI1	I				Keyboard Matrix a coordinate axis X 1.
37	TPD_CLK	I				Touch pad clock signal.
38	KBD_KI2	I				Keyboard Matrix a coordinate axis X 2.
39	RING#	I				Com port ring signal.
40	KBD_KI3	I				Keyboard Matrix a coordinate axis X 3.

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1.3.19.11 Mother Board to I/O Board (120Pin) Panasonic 2 of 3 J7-(3)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
41	HDD_HEAT_PWM	I				HDD heater power control manage.
42	KBD_KI4	I				Keyboard Matrix a coordinate axis X 4.
43	H8_RESET#	I				H8 Reset signal.
44	KBD_KI5	I				Keyboard Matrix a coordinate axis X 5.
45	LED_CLK	I				LED display clock signal.
46	KBD_KI6	I				Keyboard Matrix a coordinate axis X 6.
47	LED_DATA	I/O				LED display DATA signal.
48	KBD_KI7	I				Keyboard Matrix a coordinate axis X 7.
49	MAINON	I				System Power on.
51	LID#	O				LID Signal
52	HDD&BAT_CLK	I/O				SMbus HDD Clock
55	IDE_HDD_RST#	O				IDE HDD reset signal.
56	HDD&BAT_DATA	I/O				SMbus HDD Data
57	FIRSET	O				SIR and FIR Selection.
59	MINI_PD#	O				Mini PCI power down.
60	PCI_PME#	O				Power Management
61,69,75,77,70,72,74,82	N/A	-				NA
62	-SUSB	O				Suspend Signal

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1.3.19.11 Mother Board to I/O Board (120Pin) Panasonic 2 of 3 J7-(4)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
63	KBD_US/JP#	O				GPIO US/JP Keyboard Switch Signal
64	IGN	O				IGNITION signal power on
65	KBD_EN_EL	O				Keyboard Back Light EN/EL Signal
66	SBSPKR	O				South Bridge Speak
67	LEARNING	O				Software disable AC function
68	COM3#/TUH	O				Com3 and Touch Screen Switch Signal
71	SUSP_LED#	O				Indicate Suspend Status
73	ISA_NOGO	O				ISA Signal
76	PWROK	O				Power OK Signal
78	IDE_HDD_PWR	O				IDE Power ON/OFF Signal
79	SUSPEND#	O				Suspend Signal
80	IDE_HDD_PIRQ14	I/O				HDD IRQ
81	CRT_IN#	I				Indicate CRT Status
83	ENPBLT1	O				Enable Back Light Signal
84	SERIRQ	I/O				Serial IRQ Signal
85	MPCIACT#	I/O				Mini PCI Signal
87	LPC_PD#	O				LPC Power Down
88	ACZ_RST#	O				High Definition Audio Reset
90	ACZ_SDIN0	I/O				High Definition Audio Serial Data0
91	PCICLK_ISA_BG	O				PCI CLOCK

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1.3.19.11 Mother Board to I/O Board (120Pin) Panasonic 2 of 3 J7-(5)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
92	ACZ_M_SDIN1	I/O				High Definition Audio Serial Data1
94	ACZ_SDOUT	O				High Definition Audio Serial Data Output
95	PCI_1394_CLK	O				PCI CLOCK
96	ACZ_BIT_CLK	O				High Definition Audio CLOCK
98	ACZ_SYNC	I/O				High Definition Audio Sync
99	PCI_CLK_BAY2	O				PCI CLOCK
100	GPI_DO	I/O				GPIO Pin
102	GPO_CS	I/O				GPIO Pin
103	PCI_LPC_CLK	O				PCI CLOCK
106	GPO_DI	I/O				GPIO Pin
107	LPC_DRQ0#	I/O				LPC DMA Request
108	GPO_SK	I/O				GPIO Pin
109	LPC_FRAME#	I/O				LPC FRAM
110	LCD_ID0	I				LCD ID Signal 0
111	LPC_LAD0	I/O				LPC Address-Data 0
112	LCD_ID1	I				LCD ID Signal1
113	LPC_LAD1	I/O				LPC Address-Data 1
114	LCD_ID2	I				LCD ID Signal2
115	LPC_LAD2	I/O				LPC Address-Data 2
116	ICH7_SMB_CLK	I/O				South Bridge SMBUS CLK
117	LPC_LAD3	I/O				LPC Address-Data 3

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1.3.19.12 Mother Board to I/O Board (120Pin) Panasonic 3 of 3 J4-(1)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
1	IDE_HDD_D0					IDE Device Data
2,6,10,20,24,28,32,40,46,52,58,64,70,76,80,88,94,100,106,112,33,37,41,59,61,67,71	GND					Ground
3	IDE_HDD_D1	I/O				IDE Device Data
4	PCI_CLK_MINI	O				PCI CLOCK
5	IDE_HDD_D2	I/O				IDE Device Data
7	IDE_HDD_D3	I/O				IDE Device Data
8	PCI_CLK_CARD	O				PCI CLOCK
9	IDE_HDD_D4	I/O				IDE Device Data
11	IDE_HDD_D5	I/O				IDE Device Data
12	CRT_HSYNC	I/O				CRT Horizontal Sync. Signal
13	IDE_HDD_D6	I/O				IDE Device Data
14	CRT_VSYNC	I/O				CRT Vertical Sync. Signal
15	IDE_HDD_D7	I/O				IDE Device Data
16	CRT1_DDCDATA	I/O				CRT DDC DATA Signal
17	IDE_HDD_D8	I/O				IDE Device Data
18	CRT1_DDCCLK	O				CRT DDC CLOCK Signal

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1.3.19.12 Mother Board to I/O Board (120Pin) Panasonic 3 of 3 J4-(2)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
19	IDE_HDD_D9	I/O				IDE Device Data
21	IDE_HDD_10	I/O				IDE Device data 10
22	CRT_R	O				CRT GREEN SIGNAL
23	IDE_HDD_D11	I/O				IDE Device Data
24	IDE_HDD_D12	I/O				IDE Device data 12
26	CRT_G	O				CRT GREEN SIGNAL
27	IDE_HDD_D13	I/O				IDE Device Data
29	IDE_HDD_D14	I/O				IDE Device Data
30	CRT_B	O				CRT BLUE SIGNAL
31	IDE_HDD_D15	I/O				IDE Device Data
34,91,93,95,97,99,101,103,105,107,109,111,113,115,117,119,118,120	N/A					NA
35	IDE_HDD_P1ORD	I/O				I/O Channel Ready.
36	COM2_TXD	I/O				COM2 Transmitted data signal
38	COM2_RXD	I/O				COM2 Received data signal
39	IDE_HDD_PDIOR #	O				Disk I/O Read.
42	CLK_PCIE_LAN	O				PCI-EXPRESS Clock Positive
43	IDE_HDD_PCS1#	I/O				IDE Chip Select signal 1

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1.3.19.12 Mother Board to I/O Board (120Pin) Panasonic 3 of 3 J4-(3)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
44	CLK_PCIE_LAN#	I/O				PCI-EXPRESS CLOCK Negative
45	IDE_HDD_PCS3#	I/O				IDE Chip Select signal 3
47	IDE_HDD_PDACK#	I/O				IDE DMA Acknowledge
48	PCIE_LAN_RST	O				PCI-EXPRESS LAN Reset
49	IDE_HDD_PDREQ	I				IDE DMA Request
50	PCIE_WAKE#	I				PCI-EXPRESS Signal
51	IDE_HDD_PDROW#	I/O				IDE Write Strobe
53	IDE_HDD_PDA0	I/O				IDE Address 0
54	PCIE_TXP1	I/O				PCIE Differential Signal
55	IDE_HDD_PDA1	I/O				IDE Address 1
56	PCIE_TXN1	I/O				PCIE Differential Signal
57	IDE_HDD_PDA2	I/O				IDE Address 2
60	PCIE_RXN1	I/O				PCIE Differential Signal
62	PCIE_RXP1	I/O				PCIE Differential Signal
63	SATA_HDD_RXP0	I/O				SATA Differential Signal
65	SATA_HDD_RXN0	I/O				SATA Differential Signal
66	PCIE_TXP4	I/O				PCIE Differential Signal
68	PCIE_TXN4	I/O				PCIE Differential Signal
69	SATA_HDD_TXP0	I/O				SATA Differential Signal
71	SATA_HDD_TXN0	I/O				SATA Differential Signal
72	PCIE_RXN4	I/O				PCIE Differential Signal
74	PCIE_RXP4	I/O				PCIE Differential Signal

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1.3.19.12 Mother Board to I/O Board (120Pin) Panasonic 3 of 3 J4-(4)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
77	SATA_HDD_RXN2	I/O				SATA Differential Signal
78	32KOUT	O				EXPRESS CARD CLOCK
79	SATA_HDD_RXP2	I/O				SATA Differential Signal
82	CLK_PCIE_BAY2#	O				PCI-EXPRESS Clock Negative
83	SATA_HDD_TXN2	I/O				SATA Differential Signal
84	CLK_PCIE_BAY2	I/O				PCI-EXPRESS Clock Positive
85	SATA_HDD_TXP2	I/O				SATA Differential Signal
86	MINI_PCIE_CLK_REQ#	I/O				PCI-EXPRESS Request
89	PCIE_CLK_REQ2#	I/O				PCI-EXPRESS Request
90	PCIE_TXP5	I/O				PCIE Differential Signal
92	PCIE_TXN5	I/O				PCIE Differential Signal
96	PCIE_RXN5	I/O				PCIE Differential Signal
98	PCIE_RXP5	I/O				PCIE Differential Signal
102	PCIE_TXP6	I/O				PCIE Differential Signal
104	PCIE_TXN6	I/O				PCIE Differential Signal
108	PCIE_RXN6	I/O				PCIE Differential Signal
110	PCIE_RXP6	I/O				PCIE Differential Signal
114	CLK_PCIE_MINI_CARD#	I/O				PCI-EXPRESS Clock Negative
116	CLK_PCIE_MINI_CARD	I/O				PCI-EXPRESS Clock Positive

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1.3.19.13 Expansion Board to Board Interface-1-(1)

Item	Signal Name / Description	Power On default Direction	S0 State	S3 State	S4 State	Power plane
1	USBP6+	I/O				USB Differential Data Positive
2	PCIE_TXN3	I/O				PCIE Signal
3	USBP6-	I/O				USB Differential Data Negative
4	PCIE_TXP3	I/O				PCIE Signal
5	PCI_CLKRUN					PCI CLK running
6	PCIE_TXN2	I/O				PCIE Signal
7	LPC_FRAME#	O				LPC cycle FRAME#
8	PCIE_TXP2	I/O				PCIE Signal
9	LPC_DRQ#1	I				LPC Address
10	PCIE_RXP2	I/O				PCIE Signal
11	PCI_RST#	I				PCI Reset
12	PCIE_RXN2	I/O				PCIE Signal
13	PCI_PME#					Power Management
14	PCIE_RXP3	I				PCIE Signal
15	CLK_14.318MHZ	O				Clock
16	PCIE_RXN3	I				PCIE Signal
17	LPC_LAD0	I/O				LPC Address
18	CLK_PCIE__EXPANSION#2	I/O				PCIE Signal
19	LPC_LAD1	I/O				LPC Address
20	CLK_PCIE__EXPANSION2	I/O				PCIE Signal

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1.3.19.13 Expansion Board to Board Interface-1-(2)

Item	Signal Name / Description	Power On default Direction	S0 State	S3 State	S4 State	Power plane
22	CLK_PCIE__EXPANSION#3	I/O				PCIE Signal
23	LPC_LAD3	I/O				LPC Address
24	CLK_PCIE__EXPANSION#3	I/O				PCIE Signal
25	PCIE_WAKE#	O				PCIE Signal
26	SERIRQ	I/O				Serial IRQ
27	32KOUT	O				PCIE Signal
28	PCI_LPC_CLK	O				PCI Clock
29	SUSB#	O				Standby signal
30	LPC_PD#	O				LPC Power down
31	PWR_ON	O				System Power on
32	PCIECLKREQ1#	I				PCIE Signal
33~40	NC	-				NC
41~48	Vsys	Power				+19V
49~56	GND	Power				GND

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1.3.19.14 Expansion Board to Board Interface-2-(1)

Item	Signal Name / Description	Power On default Direction	S0 State	S3 State	S4 State	Power plane
1	PCI_AD0	I/O				PCI address/data bus
2	PCI_AD1	I/O				PCI address/data bus
3	PCI_AD2	I/O				PCI address/data bus
4	PCI_AD3	I/O				PCI address/data bus
5	PCI_AD4	I/O				PCI address/data bus
6	PCI_AD5	I/O				PCI address/data bus
7	PCI_AD6	I/O				PCI address/data bus
8	PCI_AD7	I/O				PCI address/data bus
9	PCI_AD8	I/O				PCI address/data bus
10	PCI_AD9	I/O				PCI address/data bus
11	PCI_AD10	I/O				PCI address/data bus
12	PCI_AD11	I/O				PCI address/data bus
13	PCI_AD12	I/O				PCI address/data bus
14	PCI_AD13	I/O				PCI address/data bus
15	PCI_AD14	I/O				PCI address/data bus
16	PCI_AD15	I/O				PCI address/data bus
17	PCI_AD16	I/O				PCI address/data bus
18	PCI_AD17	I/O				PCI address/data bus
19	PCI_AD18	I/O				PCI address/data bus
20	PCI_AD19	I/O				PCI address/data bus
21	PCI_AD20	I/O				PCI address/data bus
22	PCI_AD21	I/O				PCI address/data bus

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1.3.19.14 Expansion Board to Board Interface-2-(2)

Item	Signal Name / Description	Power On default Direction	S0 State	S3 State	S4 State	Power plane
24	PCI_AD23	I/O				PCI address/data bus
25	PCI_AD24	I/O				PCI address/data bus
26	PCI_AD25	I/O				PCI address/data bus
27	PCI_AD26	I/O				PCI address/data bus
28	PCI_AD27	I/O				PCI address/data bus
29	PCI_AD28	I/O				PCI address/data bus
30	PCI_AD29	I/O				PCI address/data bus
31	PCI_AD30	I/O				PCI address/data bus
32	PCI_AD31	I/O				PCI address/data bus
33	PCI_RST#	I				PCI-Reset
34	PCI_RST#	I				PCI-Reset
35	PCI_FRAME#	I/O				Bus cycle Frame
36	PCI_FRAME#	I/O				Bus cycle Frame
37	PCI_TRDY#	I/O				Bus target ready
38	PCI_TRDY#	I/O				Bus target ready
39	PCI_STOP#	I/O				Bus stop
40	PCI_STOP#	I/O				Bus stop
41	PCI_PAR	I/O				Bus parity
42	PCI_PAR	I/O				Bus parity
43	PCI_PERR#	I/O				Bus parity error indicator
44	PCI_IRDY	I/O				Bus initiator ready

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1.3.19.14 Expansion Board to Board Interface-2-(3)

Item	Signal Name / Description	Power On default Direction	S0 State	S3 State	S4 State	Power plane
46	PCI_DEVSEL#	I/O				Bus target ready
47	PCI_INTH#	I/O				Bus interrupt H
48	PCI_LOCK#	I/O				Bus lock
49	PCI_REQ5#	I				Bus request 5
50	PCI_SERR#	I/OD				Bus system error
51	PCI_GNT5#	O				Bus grant 5
52	PCI_EXPANSION_CLK	O				PCI_CLOCK
53	PCI_CBE#2	I/O				Bus commands and byte enables 2.
54	PCI_CBE#0	I/O				Bus commands and byte enables 0.
55	PCI_CBE#3	I/O				Bus commands and byte enables 3.
56	PCI_CBE#1	I/O				Bus commands and byte enables 1.

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1.3.19.15 I/O to PCMCIA Connector (180Pin) Suyin-(1)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
1,55,57,79	+5V	Power				System power +5V
2,18,54,58,66,80,174	+5VS	Power				System power +5VS
3,7,11	AGND	Power				Analogy Ground.
4,12,16,20,56,68,70,82,124,156,160,19,39,45,51,67,69,75,113,145	GND	Power				Ground
5	BAY2_MIC2_IN_L	I				BAY2 MIC Voice Input
6,8,10,134,13,15,17,77	N/A	-				N/A
9	BAY2_MIC2_IN_R	I				BAY2 MIC Voice Input
14	PCI_1394_CLK	I				PCI Clock
21	IDE_HDD_PDA0	O				IDE Device Address.
22	IDE_HDD_D0	I/O				IDE Device data.
23	IDE_HDD_PDA1	O				IDE Device Address.
24	IDE_HDD_D1	I/O				IDE Device data.
25	IDE_HDD_PDA2	O				IDE Device Address.
26	IDE_HDD_D2	I/O				IDE Device data.

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1.3.19.15 I/O to PCMCIA Connector (180Pin) Suyin-(2)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
27	IDE_HDD_PCS1#	O				IDE Device Chip Selects for 100 Range.
28	IDE_HDD_D3	I/O				IDE Device data.
29	IDE_HDD_PCS3#	O				IDE Device Chip Selects for 300 Range.
30	IDE_HDD_D4	I/O				IDE Device data.
31	IDE_HDD_PDACK#	O				IDE Device DMA Acknowledge.
32	IDE_HDD_D5	I/O				IDE Device data.
33	IDE_HDD_PDREQ	I				IDE Device DMA Request.
34	IDE_HDD_D6	I/O				IDE Device data.
35	IDE_HDD_PDIOW#	O				Disk I/O Write.
36	IDE_HDD_D8	I/O				IDE Device data.
37	IDE_HDD_RST#	I				IDE Device reset.
38	IDE_HDD_D8	I/O				IDE Device data.
40	IDE_HDD_D9	I/O				IDE Device data.
41,144	TEST POINT	-				This pin is test point.
42	IDE_HDD_D10	I/O				IDE Device data.
43	CDLED#	O				IDE Device Led display.
44	IDE_HDD_D11	I/O				IDE Device data.
46	IDE_HDD_D12	I/O				IDE Device data.
47	IDE_HDD_PDIOR#	O				Disk IO Read.
48	IDE_HDD_D13	I/O				IDE Device data.

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1.3.19.15 I/O to PCMCIA Connector (180Pin) Suyin-(3)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
49	IDE_HDD_PIO RD	I				I/O Channel Ready.
50	IDE_HDD_D14	I/O				IDE Device data.
52	IDE_HDD_D15	I/O				IDE Device data.
53	+12V	Power				+12V
59	GPRS_SPK_L	I				GPRS Voice Signal
60	BT_ACTIVE	I				BT Communication with WLAN
61	GPRS_SPK_R	I				GPRS Voice Signal
62	WLAN_ACTIVE	I				WLAN Communication with BT
63	PCI_GNT#2	O				PCI Bus grant
64	+1.8V					+1.8V
65	PCI_REQ#2	O				PCI Bus Request
71	USBP1+	I/O				USB Differential Data Positive
72	USBOC1#	I				USB Over current Signal
73	USBP1-	I/O				USB Differential Data Negative
74	PWROK	O				Power Ok Signal
76	SPK_OFF	O				Speak Off Signal
78	MINI_PD#	O				Mini PCI Power Down
81	PCI_AD31	I/O				PCI address/data bus
83	PCI_AD29	I/O				PCI address/data bus
84	PCI_AD30	I/O				PCI address/data bus
85	PCI_AD27	I/O				PCI address/data bus

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1.3.19.15 I/O to PCMCIA Connector (180Pin) Suyin-(4)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
86	PCI_AD28	I/O				PCI address/data bus
87	PCI_AD25	I/O				PCI address/data bus
88	PCI_AD26	I/O				PCI address/data bus
89	PCI_AD23	I/O				PCI address/data bus
90	PCI_AD24	I/O				PCI address/data bus
91	PCI_AD21	I/O				PCI address/data bus
92	PCI_AD22	I/O				PCI address/data bus
93	PCI_AD19	I/O				PCI address/data bus
94	PCI_AD20	I/O				PCI address/data bus
95	PCI_AD17	I/O				PCI address/data bus
96	PCI_AD18	I/O				PCI address/data bus
97	PCI_AD14	I/O				PCI address/data bus
98	PCI_AD16	I/O				PCI address/data bus
99	PCI_AD12	I/O				PCI address/data bus
100	PCI_AD15	I/O				PCI address/data bus
101	PCI_AD10	I/O				PCI address/data bus
102	PCI_AD13	I/O				PCI address/data bus
103	PCI_AD8	I/O				PCI address/data bus
104	PCI_AD11	I/O				PCI address/data bus
105	PCI_AD7	I/O				PCI address/data bus
106	PCI_AD9	I/O				PCI address/data bus
107	PCI_AD5	I/O				PCI address/data bus

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1.3.19.15 I/O to PCMCIA Connector (180Pin) Suyin-(5)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
108	PCI_AD6	I/O				PCI address/data bus
109	PCI_AD3	I/O				PCI address/data bus
110	PCI_AD4	I/O				PCI address/data bus
111	PCI_AD1	I/O				PCI address/data bus
112	PCI_AD2	I/O				PCI address/data bus
114	PCI_AD0	I/O				PCI address/data bus
115	PCI_PAR	I/O				Bus parity
116	PCI_SERR#	I/OD				Bus system error
117	PCI_LOCK#	I/O				Bus lock
118	PCI_STOP#	I/O				Bus stop
119	PCI_DEVSEL#	I/O				Device Select.
120	PCI_IRDY#	I/O				Bus initiator ready
121	PCI_PERR#	I/O				Bus parity error indicator
122	PCI_TRDY#	I/O				Bus target ready
123	PCI_FRAME#	I/O				Bus cycle Frame
125	PCI_GNT#0	O				Bus grant 0
126	PCI_INTA#	O				Bus interrupt A
127	PCI_GNT#1	O				Bus grant 1
128	PCI_INTB#	O				Bus interrupt B
129	PCI_REQ#	I				Bus request Q
130	PCI_INTC#	O				Bus interrupt C
131	PCI_REQ#1	I				Bus request 1

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1.3.19.15 I/O to PCMCIA Connector (180Pin) Suyin-(6)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
132	PCI_INTE#	O				Bus interrupt E
133	PCI_CLKRUN#	O				PCI clock Run.
135	PCI_PME#	O				Power Management
136	PCI_RST#	O				PCI Reset
137	PCI_CBE#0	O				Bus commands and byte enables 0.
138	SERIRQ	I/O				Serial IRQ
139	PCI_CBE#1	I/O				Bus commands and byte enables 1.
140	-SUSB	O				Suspend Signal
141	PCI_CBE#2	I/O				Bus commands and byte enables 2.
142	CARD_RI#	I				Card Ring Signal
143	PCI_CBE#3	I/O				Bus commands and byte enables 3.
146	VOL_ADJ	O				Voice Adjust
147	PCI_CLK_CARD	O				PCI Clock
148	SBSPKR	O				South Bridge Speak
150	MODEM_SPK	O				Modem Speak
151	PCI_CLK_MINI	O				PCI Clock
152	PCI_INTF#	O				Bus interrupt F
154	BAY2_MIC	I				Bay2 MIC Voice
155	SUSPEND#	O				Suspend Signal
157,,159,161,163	+3V					+3VS

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1.3.19.15 I/O to PCMCIA Connector (180Pin) Suyin-(6)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
158	ACZ_BIT_CLK	O				AC97 Bit Clock Input
162	ACZ_RST#	O				Audio Dock Reset
164	ACZ_SDIN0	O				Audio Serial Data In
165,167	+12VS					+12VS
166	ACZ_M_SDIN1	O				Audio Serial Data In
168	ACZ_SDOUT	O				Audio Serial Data Output
169,171	+3VS					+3VS
170	ACZ_SYNC	I/O				Audio Sync
172	MPCIACT#	I/O				
176,178	VSYS					+19V

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1.3.19.16 BAY1 Interface-(1)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
A1,A6 B15,B17 B23,B25	GND	Power				Ground
B1,B3,B5	+5VS	Power				CDROM POWER
A2	CDROM_R	I				CDROM Voice
A3,A4	CDROM_COMM	Power				Audio Grand
A5	CDROM_L	I				CDROM Voice
A7	CDLED#	O				Indicator CDROM status
A8	IDE_HDD_PCS#3	O				Chip Select signal
A9	IDE_HDD_PCS#1	O				Chip Select signal
A10	IDE_HDD_PAD2	O				Address 2
A11	IDE_HDD_PAD0	O				Address 0
A12	IDE_HDD_PAD1	O				Address 1
A13	+5VS	Power				+5VS
A14,B2 B4,B6 B10,B11 B12,B14 B16,B18 B19,B20 B22,B24 B26	NC	-				NC
A15	IDE_HDD_READY	I				I/O Ready

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1.3.19.16 BAY1 Interface-(2)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
A16	IDE_ HDD _PDIOR#	O				Read Strobe
A17	IDE_ HDD _PDIOW	O				Write Strobe
A18	IDE_ HDD _SD 15	I/O				IDE Device data 15
A19	IDE_ HDD _SD 0	I/O				IDE Device data 0
A20	IDE_ HDD _SD 14	I/O				IDE Device data 14
A21	IDE_ HDD _SD 1	I/O				IDE Device data 1
A22	IDE_ HDD _SD 13	I/O				IDE Device data 13
A23	IDE_ HDD _SD 2	I/O				IDE Device data 2
A24	IDE_ HDD _SD 12	I/O				IDE Device data 12
A25	IDE_ HDD _SD 3	I/O				IDE Device data 3
A26	IDE_ HDD _SD 11	I/O				IDE Device data 11
A27	IDE_ HDD _SD 4	I/O				IDE Device data 4
A28	IDE_ HDD _SD 10	I/O				IDE Device data 10
A29	IDE_ HDD _SD 5	I/O				IDE Device data 5
A30	IDE_ HDD _SD 9	I/O				IDE Device data 9
B7	IDE_ HDD _PDDACK#	O				DMA Acknowledge
B8	IDE_ HDD _PDDREQ	I				DMA Request
B9	USBP1+	I/O				USB Differential Data Positive
B13	USBP1-	I/O				USB Differential Data Negative
B21	CS#	O				Master device

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1.3.19.16 BAY1 Interface-(3)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
B27	IDE_HDD_SD 6	I/O				IDE Device data 6
B28	IDE_HDD_SD8	I/O				IDE Device data 8
B29	IDE_HDD_SD 7	I/O				IDE Device data 7
B30	IDE_HDD_RST#	O				Reset

1.3.19.17 BAY2 Interface (60 Pin)-(1)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
A3,B3	GND	Power				Ground
A1,B2	+5VS	Power				+5VS
B4	+3VS	Power				+3VS
B1	+12VS	Power				+12VS
A2	GPRS-SPK-R	I				GPRS Voice
A4	PCI_INTA#	I				Bus interrupt A
A5	PCI_INTB#	I				Bus interrupt B
A7	PCI_REQ#3	O				Bus request 3

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1.3.19.17 BAY2 Interface (60 Pin)-(2)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
A8	PCI_CBE#3	I/O				Bus commands and byte enables 3.
A9	PCI_CBE#2	I/O				Bus commands and byte enables 2.
A10	PCI_IRDY#	I/O				Bus initiator ready
A11	PCI_DEVSEL#	I/O				Bus target ready
A12	PCI_LOCK#	I/O				Bus lock
A13	PCI_SERR#	I/OD				Bus system error
A14	PCI_PERR#	I/O				Bus parity error indicator
A15	PCI_AD31	I/O				PCI address/data bus
A16	PCI_AD29	I/O				PCI address/data bus
A17	PCI_AD27	I/O				PCI address/data bus
A18	PCI_AD25	I/O				PCI address/data bus
A19	PCI_AD23	I/O				PCI address/data bus
A20	PCI_AD21	I/O				PCI address/data bus
A21	PCI_AD19	I/O				PCI address/data bus
A22	PCI_AD17	I/O				PCI address/data bus
A23	PCI_AD15	I/O				PCI address/data bus
A24	PCI_AD13	I/O				PCI address/data bus
A25	PCI_AD11	I/O				PCI address/data bus
A26	PCI_AD9	I/O				PCI address/data bus
A27	PCI_AD7	I/O				PCI address/data bus
A28	PCI_AD5	I/O				PCI address/data bus

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1.3.19.17 BAY2 Interface (60 Pin)-(3)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
A30	PCI_AD1	I/O				PCI address/data bus
B5	PCI_INTC#	I				Bus interrupt C
B6	PCI_INTD#	I				Bus interrupt D
B7	PCI_RST#	O				PCI-Reset
B8	PCI_GNT#3	O				Bus grant 3
B9	PCI_FRAME#	I/O				Bus cycle Frame
B10	PCI_TRDY#	I/O				Bus target ready
B11	PCI_STOP#	I/O				Bus stop
B12	PCI_PAR	I/O				Bus parity
B13	PCI_CBE#0	I/O				Bus commands and byte enables 0.
B14	PCI_CBE#1	I/O				Bus commands and byte enables 1.
B15	PCI_AD30	I/O				PCI address/data bus
B16	PCI_AD28	I/O				PCI address/data bus
B17	PCI_AD26	I/O				PCI address/data bus
B18	PCI_AD24	I/O				PCI address/data bus
B19	PCI_AD22	I/O				PCI address/data bus
B20	PCI_AD20	I/O				PCI address/data bus
B21	PCI_AD18	I/O				PCI address/data bus
B22	PCI_AD16	I/O				PCI address/data bus
B23	PCI_AD14	I/O				PCI address/data bus
B24	PCI_AD12	I/O				PCI address/data bus

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1.3.19.17 BAY2 Interface (60 Pin)-(4)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
B25	PCI_AD10	I/O				PCI address/data bus
B26	PCI_AD8	I/O				PCI address/data bus
B27	PCI_AD6	I/O				PCI address/data bus
B28	PCI_AD4	I/O				PCI address/data bus
B29	PCI_AD2	I/O				PCI address/data bus
B30	PCI_AD0	I/O				PCI address/data bus

1.3.19.18 BAY2 Interface (80 Pin)-(1)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
A2,A18 A32,B2 B28,B31	GND	Power				Ground
A20,B20	+3V	Power				+3V
A21,B26	+5V	Power				+5V
A1,A19	+5VS	Power				+5VS
B1	+3VS	Power				+3VS

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1.3.19.18 BAY2 Interface (80 Pin)-(2)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
A30,A31	Vsys	Power				+19V
A3	SERIRQ	I/O				Serial IRQ
A4	COM3_DCD#	IN				COM3 Carrier detector Signal
A5	ISA_SBHE#	O				ISA System bus high enable
A6	ISA_RSTDRV	O				ISA Signal
A7	COM3_DSR#	IN				COM3 Data set ready signal
A8	ISA_IOW#	I/O				ISA I/O Write
A9	COM1CTS#	IN				COM3 Clear to send signal
A10	ISA_DREQ0	I/O				ISA DMA Request 0
A11	ISA_DREQ3	I/O				ISA DMA Request 3
A12	ISA_DREQ5	I/O				ISA DMA Request 5
A13	ISA_TC	I/O				ISA Terminal count
A14	COM3RXD	IN				COM3 Received data signal
A15	ISA_IRQ4	I				ISA Interrupt Request 4
A16	ISA_IRQ10	I				ISA Interrupt Request 10
A17	ISA_IRQ15	I				ISA Interrupt Request 15
A22	ISA_SD0	I/O				ISA Data bit 0
A23	ISA_SD2	I/O				ISA Data bit 2
A24	ISA_SD4	I/O				ISA Data bit 4
A25	ISA_SD6	I/O				ISA Data bit 6
A26	WLAN_ACTIVE	I/O				Wireless LAN signal
A27	RS232_OFF	O				RS232 Switch

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1.3.19.18 BAY2 Interface (80 Pin)-(3)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
A28	COM3RI#	IN				COM3 Ring indicator signal
A29	BAY2_MIC	I				BAY2 Microphone voice
A33	ISA_SA0	I/O				ISA Address bit 0
A34	ISA_SA2	I/O				ISA Address bit 2
A35	ISA_SA4	I/O				ISA Address bit 4
A36	ISA_SA6	I/O				ISA Address bit 6
A37	ISA_SA8	I/O				ISA Address bit 8
A38	ISA_SA10	I/O				ISA Address bit 10
A39	ISA_SA12	I/O				ISA Address bit 12
A40	ISA_SA14	I/O				ISA Address bit 14
B3	GPRS-SPK-L	O				GPRS Voice
B4	PCI_CLKRUN#	O				PCI CLK running
B5	ISA_MEMR#	O				ISA Memory Read
B6	COM3RTS#	O				COM3 Request to send signal
B7	ISA_AEN	O				ISA Address Latch Enable
B8	ISA_IOR#	I				ISA /O Read
B9	ISA_IOCHRDY	I				ISA I/O Channel ready
B10	COM3TXD	O				COM3 Transmitted data signal
B11	ISA_DACK0#	O				ISA DMA Acknowledge 0
B12	COM3DTR#	O				COM3 Data terminal ready signal
B13	ISA_DACK5#	O				ISA DMA Acknowledge 5

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1.3.19.18 BAY2 Interface (80 Pin)-(4)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
B14	ISA_IRQ3	I				ISA Interrupt Request 3
B15	ISA_IRQ5	I				ISA Interrupt Request 5
B16	ISA_IRQ7	I				ISA Interrupt Request 7
B17	ISA_IRQ9	I				ISA Interrupt Request 9
B18	ISA_IRQ11	I				ISA Interrupt Request 11
B19	B2MODSPK	I				BAY2 Modem Speak
B21	PCI_PME#	O				Power Mangement
B22	ISA_SD1	I/O				ISA Data bit 1
B23	ISA_SD3	I/O				ISA Data bit 3
B24	ISA_SD5	I/O				ISA Data bit 5
B25	ISA_SD7	I/O				ISA Data bit 7
B27	BT_ACTIVE	O				Blue Tooth Controller Signal
B29	USBP5+	I/O				USB Differential Data +
B30	USBP5-	I/O				USB Differential Data -
B32	ISA_SA1	I/O				ISA Address bit 1
B33	ISA_SA3	I/O				ISA Address bit 3
B34	ISA_SA5	I/O				ISA Address bit 5
B35	ISA_SA7	I/O				ISA Address bit 7
B36	ISA_SA9	I/O				ISA Address bit 9
B37	ISA_SA11	I/O				ISA Address bit 11
B38	ISA_SA13	I/O				ISA Address bit 13
B39	ISA_SA15	I/O				ISA Address bit 15
B40	ISA_SA16	I/O				ISA Address bit 16

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1.4 Electrical Characteristic

1.4.1 ICH7-M GPI/O Pin Define-(1)

Item	Multi. Func./Note	Signal Name / Descriptio	Power On default Direction	S0 State	S3 State	S4 State	Power plane
0	PM_BMBUSY#	GPIO0					
1	PCI_REQ5#(Reserved)	GPIO1/REQ5#					
2	PCI_INTE#	GPIO2/PIRQE#					
3	PCI_INTF#	GPIO3/PIRQF#					
4	PCI_INTG#	GPIO4/PIRQG#					
5	PCI_INTH#	GPIO5/PIRQH#					
6	GPO_DI	GPIO6					
7	SCI#	GPIO7					
8	EXTSMI#	GPIO8					
9	SUSPEND#	GPIO9					
10	ISA_NOGO	GPIO10					
11	GPO_CS	GPIO11/SMBALERT					
12	MPCIACT#	GPIO12					
13	WAKE_UP#	GPIO13					
14	KBD_EN_EL	GPIO14					
15	IDE_HDD_RST#	GPIO15					

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1.4.1 ICH7-M GPI/O Pin Define-(2)

Item	Multi. Func./Note	Signal Name / Description	Power On default Direction	S0 State	S3 State	S4 State	Power
							plane
16	DPRSLPVR	GPIO16/DP RSLPVR					
17	PCI_GNT5#	GPIO17/GN T5#					
18	STOP_PCI#	GPIO18/STP PCI#					
19	Reserved	GPIO19/ST A1GP					
20	STOP_CPU#	GPIO20/STP CPU#					
21	SATA0_R0	GPIO21/ST A0GP					
22	PCI_REQ4#	GPIO22/RE Q4#					
23	LPC_DRQ#1	GPIO23					
24	GPI_DO	GPIO24					
25	GPO_SK	GPIO25					
26	T/P	GPIO26/EL_ RSVD					
27	T/P	GPIO27/EL_ STATE0					
28	T/P	GPIO28/EL_ STATE0					
29	USBOC5#(Reserved)	GPIO29					
30	USBOC6#(Reserved)	GPIO30					
31	USBOC7#(Reserved)	GPIO31					
32	CLKRUN#	GPIO32					

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1.4.1 ICH7-M GPI/O Pin Define-(3)

Item	Multi. Func./Note	Signal Name / Descriptio	Power On default Direction	S0 State	S3 State	S4 State	Power plane
34	ENABKL_MSK#	GPIO34					
35	SATACLKREQ#	GPIO35					
36	SATA0_R2	GPIO36					
37	T/P	GPIO37					
38	CRT_IN#	GPIO38					
39	KBD_US/JP#	GPIO39					
40	NOT Implemented	GPIO40~47					
41	PCI_GNT4#	GPIO48					

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1.4.1 Keyboard Controller Pin Define-(1)

PIN	Port	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Connect to	Description
1	/RES	H8_RESET#	I					
2	XTAL	XTAL	I					
3	EXTAL	EXTAL	I					
4	VCCB	VCCB	I					
5	MD1	H8_MODE1	I					
6	MD0	H8_MODE0	I					
7	/NMI	H8_SUSB	I					
8	/STBY/FVPP	H8_STBY#	I					
9	VCC1	VCC1	I					
10	PA7/KEYIN15	H8_RSMRS T	O					
11	PA6/KEYIN14	DIS_CHG	O					
12	P52/SCK0	BAT_CLK_ H8	I/O					
13	P51/RXD0	RSTCHG#	I/O					
14	P50/TXD0	BA Y2_ GPIO	I/O					
15	VSS4	VSS4	I					
16	P97/WAIT/SDA	BAT_DAT A_H8	I					
17	P96/0	G_SENSOR #	O					
18	P95/AS	H8_SB_PW RBTN#	O					
19	P94/WR	BATMSL0	O					
20	PA5/KEYIN13	USE_B	O					

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1.4.1 Keyboard Controller Pin Define-(2)

PIN	Port	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Connect to	Description
21	PA4/KEYIN12	USE_A	O					
22	P93/RD	H8_THRM#	O					
23	P92/IRQ0	H8_LID#	I					
24	P91/IRQ1/EIOW	H8_POWER_BTN#	I					
25	P90/IRQ2/ESC2	H8_SUSC	I					
26	P60/KEYIN0/FTC1	KBD_KI0	I					
27	P61/KEYIN1/FTOA	KBD_KI1	O					
28	P62/KEYIN2/FTIA	KBD_KI2	I					
29	P63/KEYIN3/FTIB	KBD_KI3	I					
30	PA3/KEYIB11	TPD_DAT_A	O					
31	PA2/KEYIN10	TPD_CLK	O					
32	P64/KEYIN4/FTIC	KBD_KI4	I					
33	P65/KEYIN5/FTID	KBD_KI5	I					
34	P66/KEYIN6/IRQ6	KBD_KI6	O					
35	P67/KEYIN7/IRQ7	KBD_KI7	I					
36	AVREF	AVREF	I					
37	AVCC	AVCC	I					
38	P70/AN0	VBATT3	I					
39	P71/AN1	VBATT1	I					
40	P72/AN2	VBATT2	I					
41	P73/AN3	SEN_DDR	I					

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1.4.1 Keyboard Controller Pin Define-(3)

PIN	Port	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Connect to	Description
42	P74/AN4	SEN_3V	I					
43	P75/AN5	SEN_VCOR E	I					
44	P76/AN6/DA0	VOL_ADJ	I					
45	P77/AN7/DA1	BLADJ	I					
46	AVSS	AVSS	I					
47	PA1/KEYIN9	RING#	O					
48	PA0/KEYIN8	ADEN#	O					
49	P40/TMCIO	PWROK	I					
50	P41/TMO0	BATMSL1	O					
51	P42/TMRI0	H8_SMB_D ATA	I					
52	P43/TMC11/IRQ1	H8_SCI	I					
53	P44/TMO1/IRQ1	H8_DBG_C LK	O					
54	P45/TMRI1/IRQ1	IGN	I					
55	P46/PW0	PWR_ON	O					
56	P47/PW1	HDD_HEA T_PWM	O					
57	PB7/XDB7	LED_DATA	I/O					
58	PB6/XDB6	LED_CLK	I/O					
59	VCC2	VCC2	I					
60	P27/A15	KEY BD MATRIX : KO15	O					

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1.4.1 Keyboard Controller Pin Define-(4)

PIN	Port	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Connect to	Description
61	P26/A14	KEY BD MATRIX : KO14	O					
62	P25/A13	KEY BD MATRIX : KO13	O					
63	P24/A12	KEY BD MATRIX : KO12	O					
64	P23/A11	KEY BD MATRIX : KO11	O					
65	P22/A10	KEY BD MATRIX : KO10	O					
66	P21/A9	KEY BD MATRIX : KO9	O					
67	P20/A8	KEY BD MATRIX : KO8	O					
68	PB5/XDB4	SUSP_LED	I/O					
69	PB4/XDB4	LEARNING	I/O					
70	VSS1	VSS1	I					
71	VSS2	VSS2	I					
72	P17/A7	KEY BD MATRIX : KO7	O					

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1.4.1 Keyboard Controller Pin Define-(5)

PIN	Port	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Connect to	Description
73	P16/A6	KEY BD MATRIX : KO6	O					
74	P15/A5	KEY BD MATRIX : KO5	O					
75	P14/A4	KEY BD MATRIX : KO4	O					
76	P13/A3	KEY BD MATRIX : KO3	O					
77	P12/A2	KEY BD MATRIX : KO2	O					
78	P11/A1	KEY BD MATRIX : KO1	O					
79	P10/A0	KEY BD MATRIX : KO0	O					
80	PB3/XDB3	H8_DBG_DATA	I/O					
81	PB2/XDB2	RCIN#	I/O					
82	P30/HDB0/D0	LAD0	I/O					
83	P31/HDB1/D1	LAD1	I/O					
84	P32/HDB2/D2	LAD2	I/O					
85	P33/HDB3/D3	LAD3	I/O					

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1.4.1 Keyboard Controller Pin Define-(6)

PIN	Port	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Connect to	Description
86	P34/HDB4/D4	FRAME#	I/O					
87	P35/HDB5/D5	PLT_RST#	I/O					
88	P36/HDB6/D6	PCI_H8_CLK	I/O					
89	P37/HDB7/D7	SERIRQ	I/O					
90	PB1/XDB1	H8_WAKEUP#	I/O					
91	PB0/XDB0	EXTSMI#	I/O					
92	VSS3	VSS3	I					
93	P80/HA0	IDE_HDD_PWR	I/O					
94	P81/GA20	A20GATE	I/O					
95	P82/CLKRUN#	PCI_CLKRUN	I/O					
96	P83/PLCPD#	LPC_PD#	I/O					
97	P84/IRQ2/TXD1	H8_TX	I					
98	P85/IRQ4/RXD1	H8_RX	I					
99	P86/IRQ5/SCK1	H8_SMB_CLK	I					
100	/RESO	N/A	O					

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1.5 Version handling

PN	DECS.	REV.
411119000004	TF041-TH-PWA;PWA-A790,M/B	R00
411119000001	TF041-TH-PWA;PWA-A790,I/O BD	R00
411119000010	TF041-TH- PWA;PWA-A790,PCMCIA BD	R00
411119000007	TF041-TH-PWA;PWA-A790,LED&SW BD	R00
411119000013	TF041-TH-PWA;PWA-A790 BATT3 TRANS BD	R00
411119000016	TF041-TH-PWA;PWA-A790 CAR ADAPTER DEMO BD	R00
411119000019	TF041-TH-PWA;PWA-A790 BATTERY CHARGER BD	R00
411119000032	TF041-TH-PWA;PWA-A790,SATA HDD TRANS BD	R00
411119000025	TF041-TH-PWA;PWA-A790,TOUCH SCREEN BD	R00
411119000029	TF041-TH-PWA;PWA-A790,TOUCH PAD SW BD	R00
411119000035	TF041-TH-PWA;PWA-A790,BAY2 TRANS BD	R00
411119000038	TF041-TH-PWA;PWA-A790 CAR ADAPTER BD	R00
411119000041	TF041-TH-PWA;PWA-A790 M/B WITHOUT ATI M54	R00
411119000044	TF041-TH-PWA;PWA-A790 FINGER PRINT BD	R00

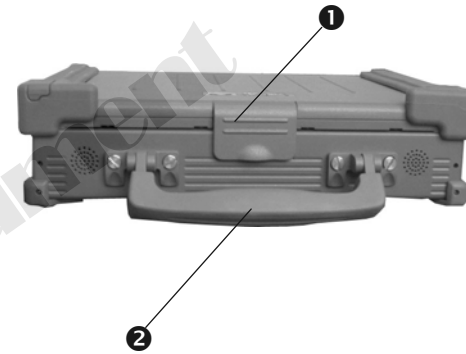
A790 N/B Maintenance

2. System View and Disassembly

2.1 System View

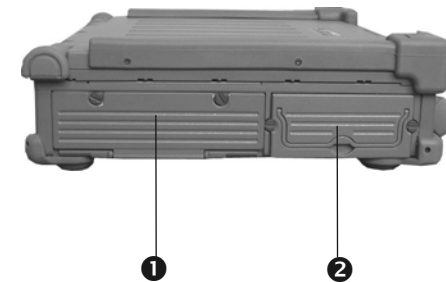
2.1.1 Front View

- ❶ Opening Latch
- ❷ Carrying Handle



2.1.2 Left-side View

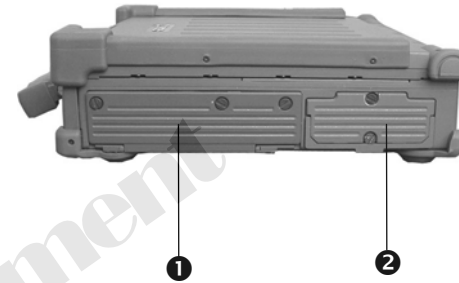
- ❶ Bay 2/Access Door
- ❷ Removable Primary Battery/Access Door



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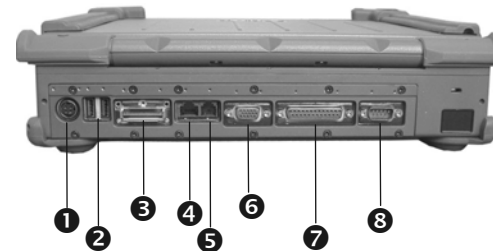
2.1.3 Right-side View

- ❶ X-bay Connector/Access Door
- ❷ Removable Hard Disk Drive Module/Access Door



2.1.4 Rear View

- ❶ Power Connector
- ❷ USB Port*2
- ❸ Port Replicator Port
- ❹ RJ45 Connector
- ❺ RJ11 Connector
- ❻ VGA Connector
- ❼ Printer Connector
- ❽ Serial Connector



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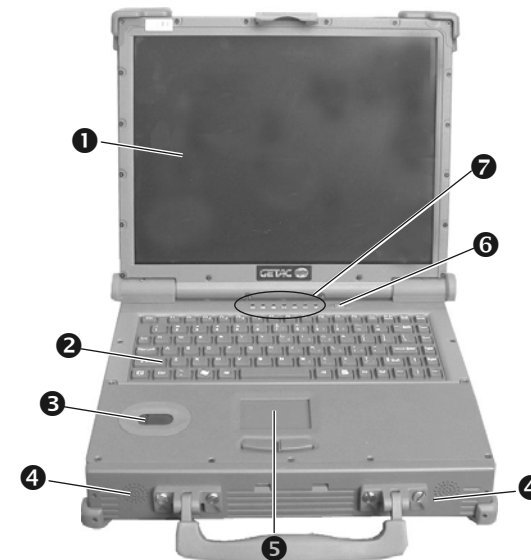
2.1.5 Bottom View

- ❶ Thermal pad



2.1.6 Top-open View

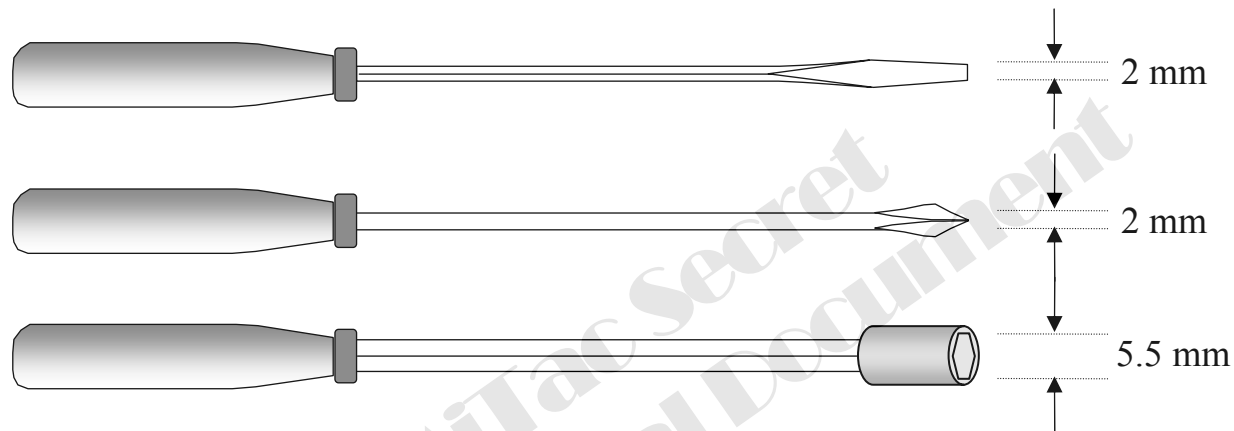
- ❶ LCD Screen
- ❷ Keyboard
- ❸ Finger Print
- ❹ Speaker
- ❺ Touch Pad
- ❻ Power Button
- ❼ LED indicator



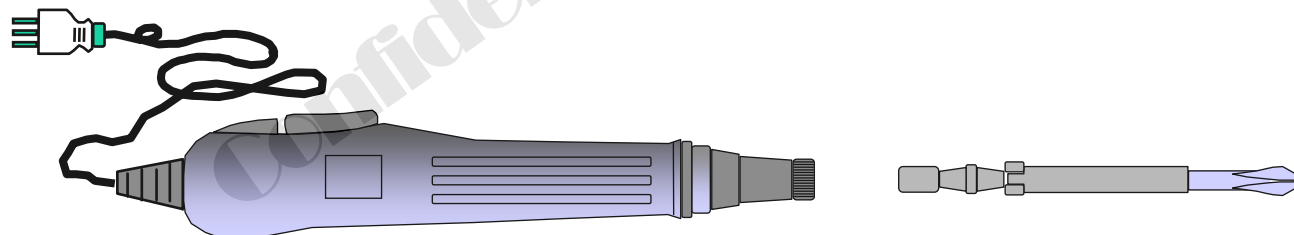
A790 N/B Maintenance

2.2 Tools Introduction

1. Screw driver with bit size for notebook assembly & disassembly.



2. Auto screw driver for notebook assembly & disassembly.



Bit Size

#0

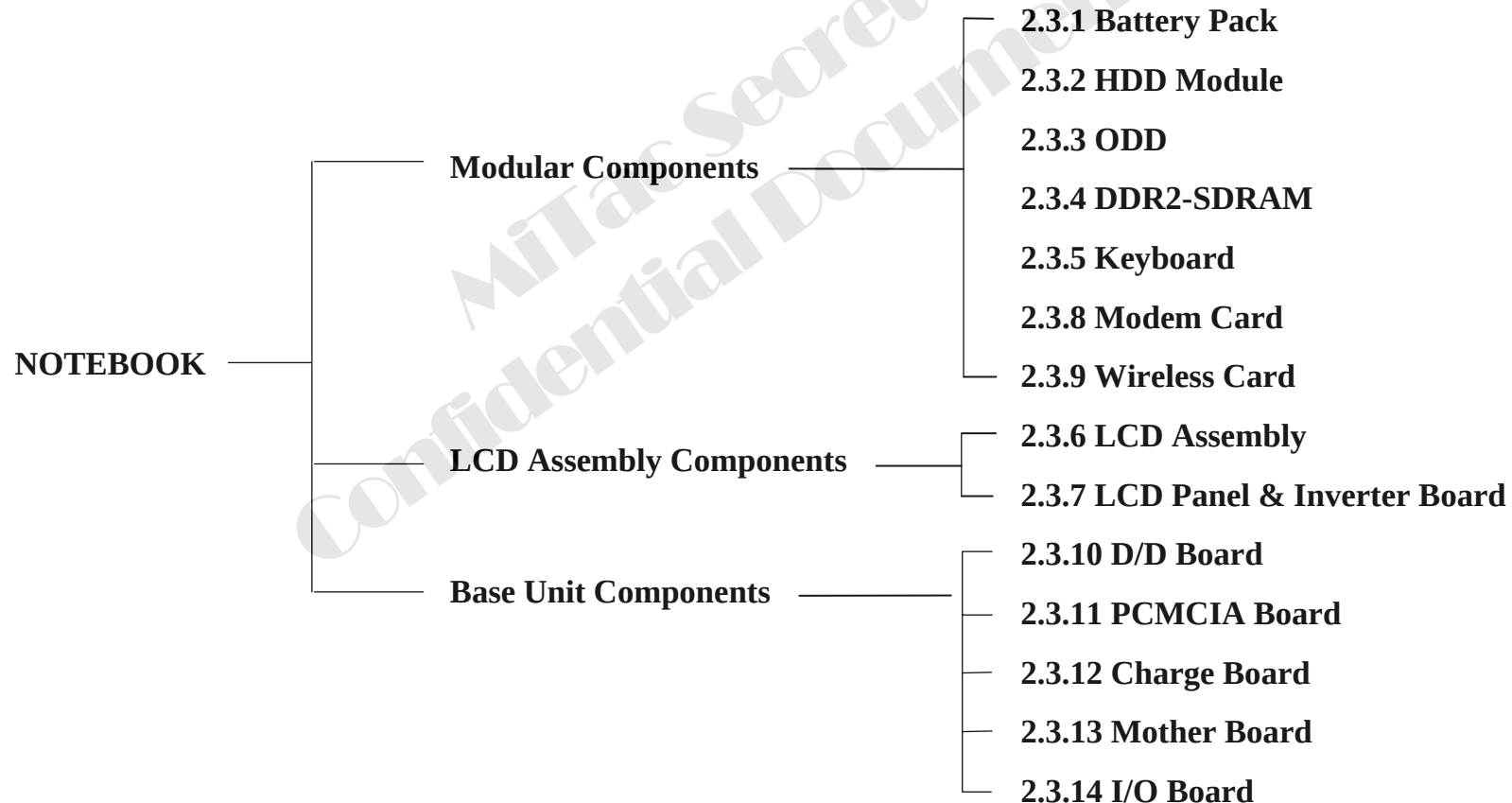
Screw Size	Tooling	Tor.	Bit Size
1. M2.0	Auto Screwdriver	2.0-2.5 kg/cm2	#0

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2.3 System Disassembly

The section discusses at length each major component for disassembly/reassembly and show corresponding illustrations. Use the chart below to determine the disassembly sequence for removing components from the notebook.

NOTE: Before you start to install/replace these modules, disconnect all peripheral devices and make sure the notebook is not turned on or connected to AC power.



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2.3.1 Battery Pack

Disassembly

1. Loosen the battery door two shoulder screws and open the door. (Figure 2-1)
2. Pull the battery out. (Figure 2-2)



Figure 2-1 Remove two screws



Figure 2-2 Pull the battery out

Reassembly

1. Install battery.
2. Close the Battery door then secured two shoulder screws.

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2.3.2 HDD Module

Disassembly

1. Remove the battery pack . (See section 2.3.1 Disassembly)
2. Then loosen the HDD box's two shoulder screws. (Figure 2-3)
3. Pull the HDD box out. (Figure 2-4)



Figure 2-3 Remove two screws



Figure 2-4 Pull the HDD box out

Reassembly

1. Install the HDD box.
2. Secured the two shoulder screws.
3. Replace battery pack. (Refer to section 2.3.1 Reassembly)

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2.3.3 ODD

Disassembly

1. Remove the battery pack . (See section 2.3.1 Disassembly)
2. Loosen the ODD door three shoulder screws and open the door. (Figure 2-5)
3. Push block ejector handle then pull out the handle outward about 3 cm. (Figure 2-6)
4. Take out ODD driver.



Figure 2-5 Remove three screws

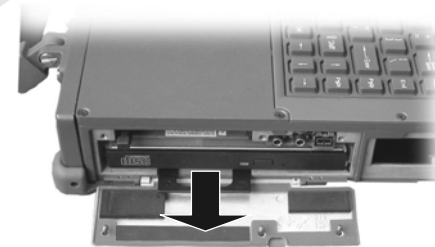


Figure 2-6 Push block ejector handle

Reassembly

1. Install ODD driver .
2. Push block ejector handle to oppose direction.
3. Close the ODD door then secured three shoulder screws.
4. Replace battery pack. (Refer to section 2.3.1 Reassembly)

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2.3.4 DDR2-SDRAM

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (See section 2.3.1 Disassembly)
2. Remove twenty screws fastening the thermal pad . (Figure 2-7)
3. Pull the retaining clips outwards (❶) and remove the DDR2-SDRAM (❷). (Figure 2-8)



Figure 2-7 Remove twenty screws

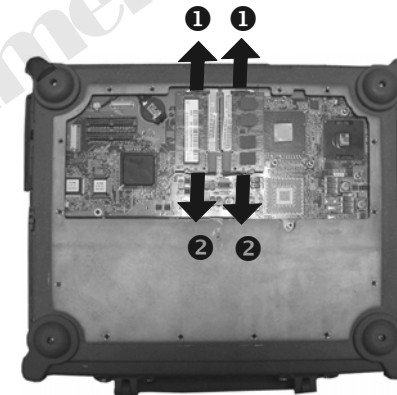


Figure 2-8 Remove the DDR2-SDRAM

Reassembly

1. To install the DDR2, match the DDR2's notched part with the socket's projected part and firmly insert the DDR2-SDRAM into the socket at 20-degree angle. Then push down until the retaining clips lock the DDR2 into position.
2. Replace the thermal pad and secure with twenty screws.
3. Replace the battery pack. (See section 2.3.1 Reassembly)

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2.3.5 Keyboard

Disassembly

1. Remove battery pack and all peripheral device.
2. Remove two rubber screw covers, two screws and two hinge rubber caps, and remove nine screws, take out of the cover (Figure 2-9)
3. Remove five screws then open the chassis cover. (Figure 2-10)



Figure 2-9 Remove nine screws

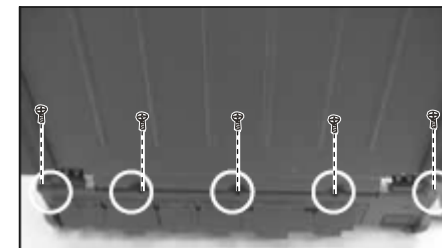


Figure 2-10 Remove five screws

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4. Remove twenty screws. (Figure 2-11)
5. Slightly lift up the keyboard, then disconnect the cable from the system board, then separate the keyboard. (Figure 2-12)

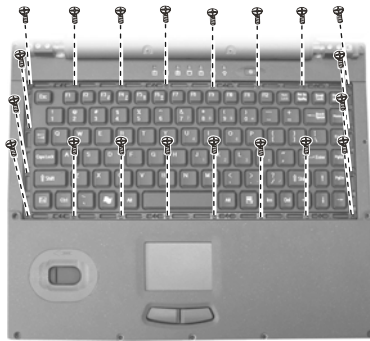


Figure 2-11 Remove twenty screws

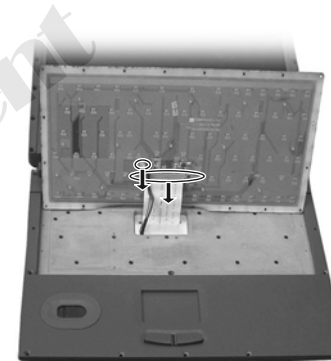


Figure 2-12 Lift the keyboard

Reassembly

1. Reconnect the keyboard cable and fit the keyboard back into place.
2. Secure with twenty screws and replace the cover .
3. Secured all screws, hinge holder and hinge rubber.
4. Remove all peripheral device.
5. Replace battery pack. (Refer to section 2.3.1 Reassembly)

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2.3.6 LCD ASSY

Disassembly

1. Remove the battery pack, hard disk drive, ODD, DDR2 and keyboard (See sections 2.3.1, 2.3.2, 2.3.3, 2.3.4, and 2.3.5 Disassembly)
2. Remove the keyboard cable. (Figure 2-13)
3. Remove the three cable , wireless wire, and two screw cap, you can lift up the LCD ASSY from base unit. (Figure 2-14)



Figure 2-13 Remove the cable

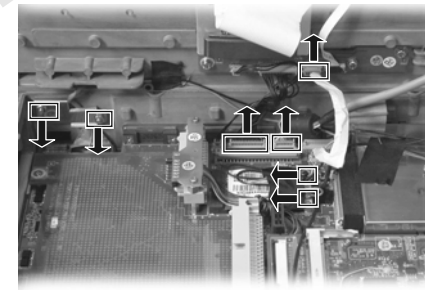


Figure 2-14 Lift up LCD ASSY

Reassembly

1. Attach the LCD assembly to the base unit and secure with two screws, reconnect wireless wire and three cables
2. Reconnect keyboard cable.
3. Replace keyboard and all peripheral device. (Refer to sections 2.3.5, 2.3.4, 2.3.3, 2.3.2 Reassembly).
4. Replace battery pack. (Refer to section 2.3.1 Reassembly)

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2.3.7 LCD Panel & Inverboard

Disassembly

1. Remove the battery pack, keyboard and LCD ASSY (See sections 2.3.1, 2.3.5 and 2.3.6 Disassembly)
2. Remove twenty screws of LCD cover. (Figure 2-15)
3. Lift up the LCD cover remove two screws fastening the inverter board, and disconnect two cable, then free the inverter board . (Figure 2-16)

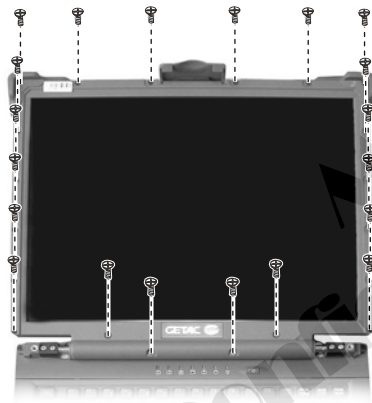


Figure 2-17 Remove LCD cover



Figure 2-18 Remove two screws and disconnect two cable

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4. Disconnect the cable to free the LCD panel. (Figure 2-17)



Figure 2-17 Free the LCD panel

Reassembly

1. Replace the LCD panel into LCD housing .
2. Fit the inverter board back into place and secure with two screws, reconnect two cables.
3. Fit the LCD cover and secure with twenty screws .
4. Replace the LCD assembly, keyboard, and battery pack. (See sections 2.3.6, 2.3.5 and 2.3.1 Reassembly)

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2.3.8 Modem Card

Disassembly

1. Remove the battery pack, hard disk drive, ODD, DDR2, keyboard, LCD assembly (See sections 2.3.1, 2.3.2, 2.3.3, 2.3.4, 2.3.5, 2.3.6 Disassembly)
2. Remove two screws fastening the modem card and disconnect the modem cable, then remove the modem card. (Figure 2-18)



Figure 2-18 Remove the modem card

Reassembly

1. To install the modem card and secure with two screws, then reconnect the modem cable.
2. Replace LCD assembly, keyboard, DDR2, ODD, HDD and battery pack. (Refer to previous section reassembly)

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2.3.9 Wireless Card

Disassembly

1. Remove the battery pack, hard disk drive, ODD, DDR2, keyboard, LCD assembly and modem.(See sections 2.3.1, 2.3.2, 2.3.3, 2.3.4, 2.3.5, 2.3.6 and 2.3.8 Disassembly)
2. Remove two screws fastening the wireless card and, then remove the modem card. (Figure 2-19)



Figure 2-19 Remove the wireless card

Reassembly

1. To install the wireless card and secure with two screws.
2. Replace modem, LCD assembly, keyboard, DDR2, ODD, HDD and battery pack. (Refer to previous section reassembly)

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2.3.10 D/D Board

Disassembly

1. Remove the battery pack, hard disk drive, ODD, DDR2, keyboard, LCD assembly, modem and wireless card.
(See sections 2.3.1, 2.3.2, 2.3.3, 2.3.4, 2.3.5, 2.3.6, 2.3.8 and 2.3.9 Disassembly)
2. Remove three screws fastening the D/D board. (Figure 2-20)
3. Disconnect the cable to free the D/D board. (Figure 2-21)

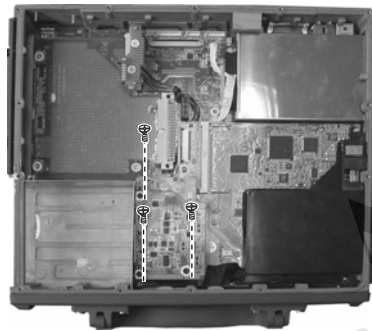


Figure 2-20 Remove three screws



Figure 2-20 Free the D/D board

Reassembly

1. Reconnect the D/D board cable and fit the D/D board back into place.
2. Secure with three screws.
3. Replace wireless card, modem, LCD assembly, keyboard, DDR2, ODD, HDD and battery pack. (Refer to previous section reassembly)

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2.3.11 PCMCIA Board

Disassembly

1. Remove the battery pack, hard disk drive, ODD, DDR2, keyboard, LCD assembly, modem and wireless card, D/D board. (See sections 2.3.1, 2.3.2, 2.3.3, 2.3.4, 2.3.5, 2.3.6, 2.3.8, 2.3.9 and 2.3.10 Disassembly)
2. Remove the cover of PCMCIA slot and two speak cable. (Figure 2-22)
3. Remove three screws then free the PCMCIA board. (Figure 2-23)

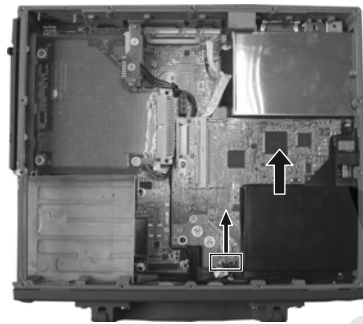


Figure 2-22 Remove the cove and cable



Figure 2-23 Free the PCMCIA board

Reassembly

1. Fit the PCMCIA board back into place secure with three screws.
2. Replace PCMCIA cover.
3. Replace D/D board, wireless card, modem, LCD assembly, keyboard , DDR2, ODD, HDD and battery pack. (Refer to previous section reassembly)

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2.3.12 Charge Board

Disassembly

1. Remove the battery pack, hard disk drive, ODD, DDR2, keyboard, LCD assembly, modem and wireless card, D/D board, PCMCIA board. (See sections 2.3.1, 2.3.2, 2.3.3, 2.3.4, 2.3.5, 2.3.6, 2.3.8, 2.3.9, 2.3.10 and 2.3.11 Disassembly)
2. Remove the plastic and three screws then free the charge board. (Figure 2-24)

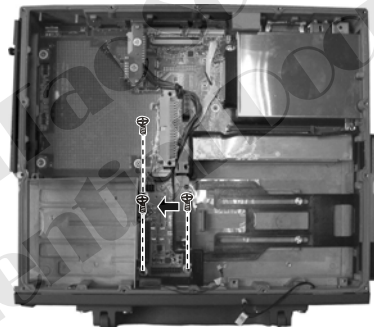


Figure 2-24 Remove the cover

Reassembly

1. Fit the charge board back into place secure with three screws.
2. Replace the plastic.
3. Replace PCMCIA board, D/D board wireless card, modem, LCD assembly, keyboard, DDR2, ODD, HDD and battery pack. (Refer to previous section reassembly)

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2.3.13 Mother Board

Disassembly

1. Remove the battery pack, hard disk drive, ODD, DDR2, keyboard, LCD assembly, modem and wireless card, D/D board, PCMCIA board, charge board. (See sections 2.3.1, 2.3.2, 2.3.3, 2.3.4, 2.3.5, 2.3.6, 2.3.8, 2.3.9, 2.3.10, 2.3.11 and 2.3.12 Disassembly)
2. Remove two screws and eight hex nuts fastening the housing. (Figure 2-25)
3. Remove three screws free the mother board. (Figure 2-26)

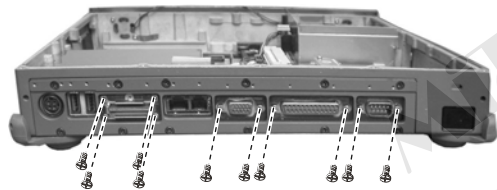


Figure 2-25 Remove two screws and eight hex nuts



Figure 2-26 Remove three screws

Reassembly

1. Fit the mother board back into place secure with three screws.
2. Secure with two screws and eight hex nuts fasten the housing.
3. Replace charge board, PCMCIA board, D/D board wireless card, modem, LCD assembly, keyboard , DDR2, ODD, HDD and battery pack. (Refer to previous section reassembly)

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2.3.14 I/O Board

Disassembly

1. Remove the battery pack, hard disk drive, ODD, DDR2, keyboard, LCD assembly, modem and wireless card, D/D board, PCMCIA board, charge board, Mother board. (See sections 2.3.1, 2.3.2, 2.3.3, 2.3.4, 2.3.5, 2.3.6, 2.3.8, 2.3.9, 2.3.10, 2.3.11, 2.3.12 and 2.3.13 Disassembly)
2. Remove five screws free the I/O board. (Figure 2-27)

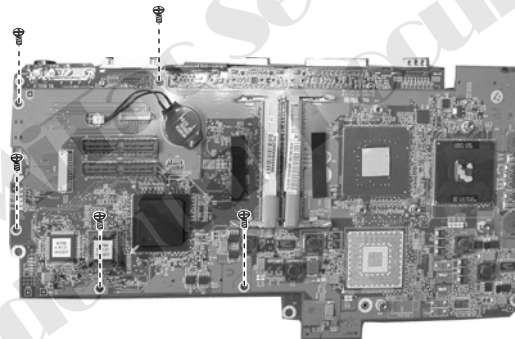


Figure 2-27 Free the I/O board

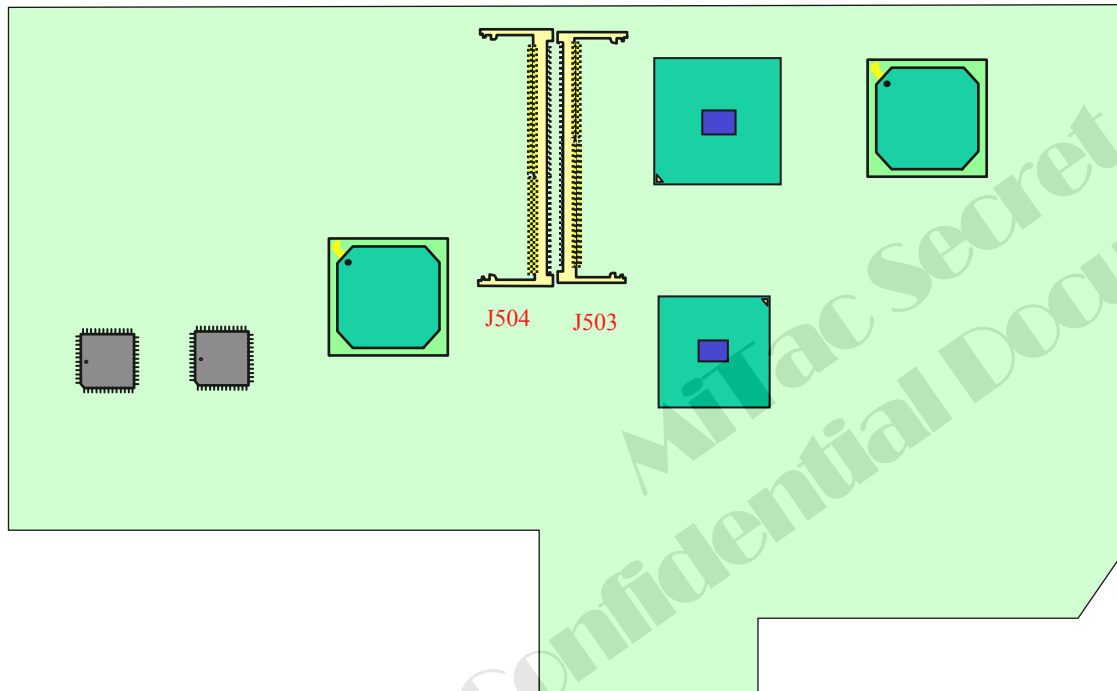
Reassembly

1. Fit the I/O board back into place secure with five screws.
2. Replace mother board, charge board, PCMCIA board, D/D board wireless card, modem, LCD assembly, keyboard, DDR2, ODD, HDD and battery pack. (Refer to previous section reassembly)

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3. Definition & Location of Connectors/Switches

3.1 Mother Board

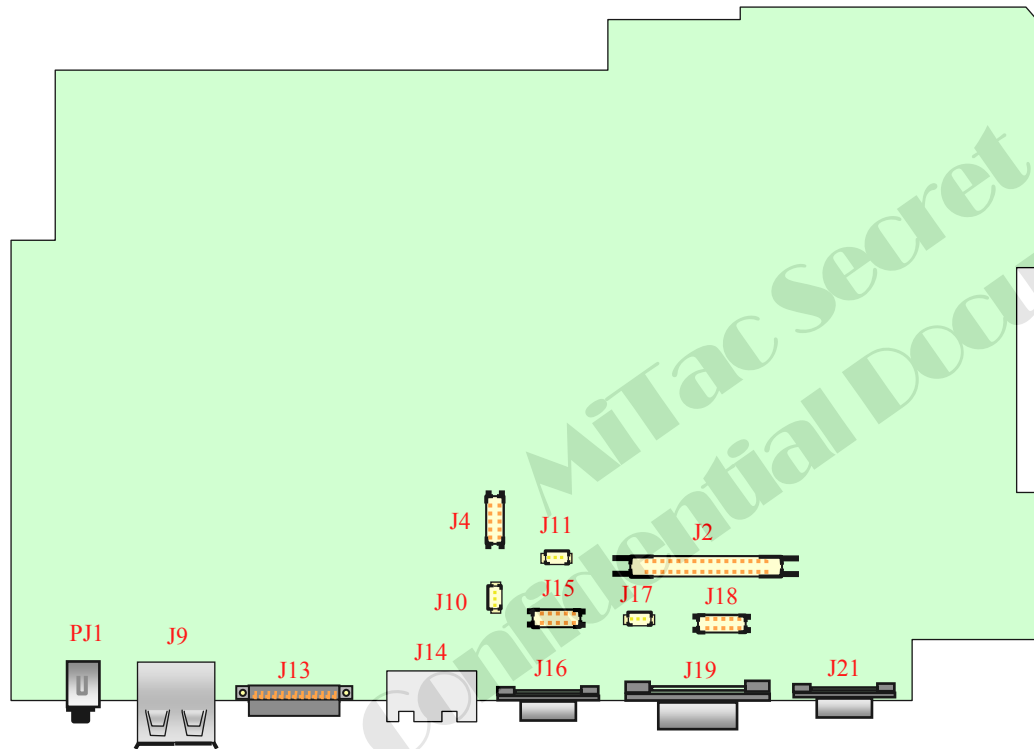


➤ J503, J504 : DDR2 SO-DIMM Socket

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3. Definition & Location of Connectors/Switches

3.2 I/O Board (Side A)

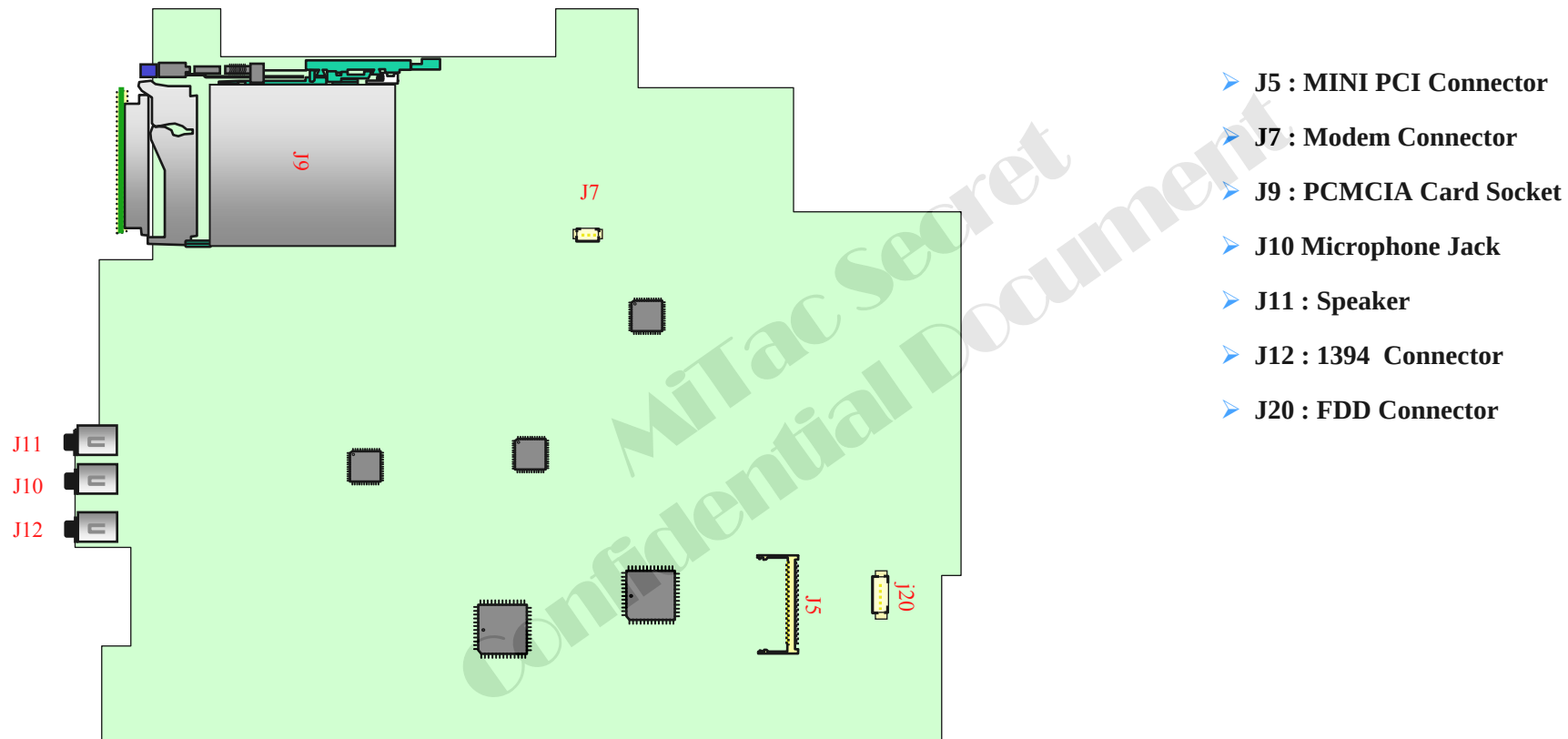


- PJ1 : Power Jack
- J4 : HDD Connector
- J10 : MDC Jump Wire Connector
- J11 : Finger Printer Connector
- J12 : Keyboard Connector
- J13 : Port Replicator Connector
- J14 : RJ45/RJ11 Connector
- J15 : Touch Screen Connector
- J16 : External VGA Connector
- J17 : Inverter Connector
- J18 : LED Board Connector
- J19 : LPT Connector
- J21 : RS232 COM1 Connector

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3. Definition & Location of Connectors/Switches

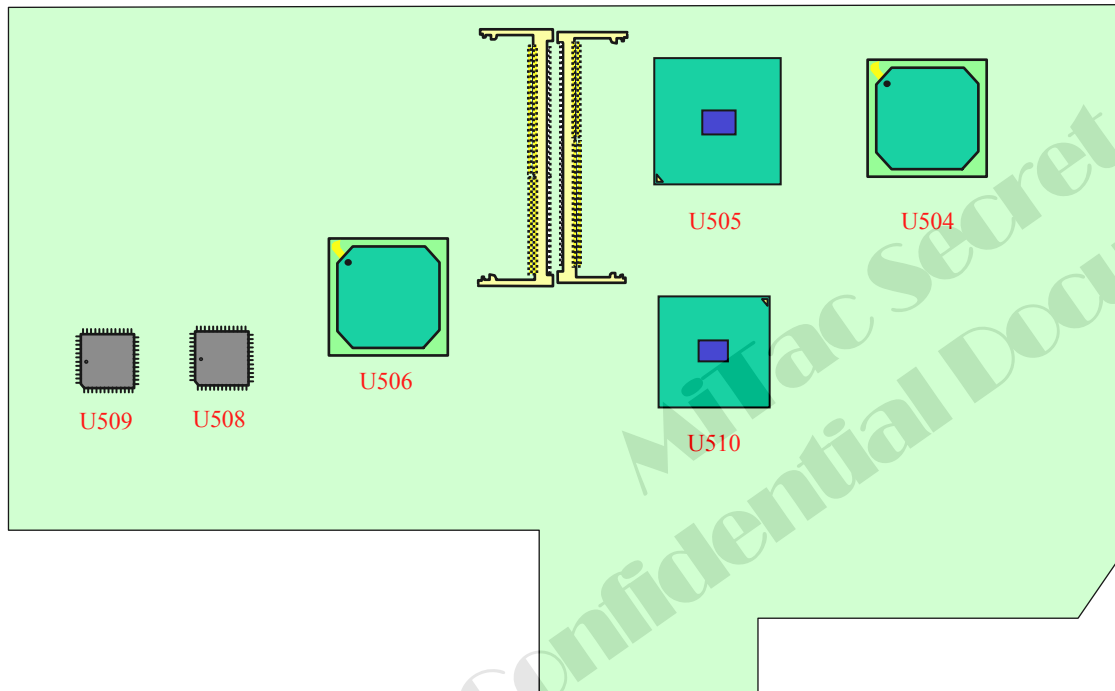
3.3 PCMCIA Board



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4. Definition & Location of Major Components

4.1 Mother Board (Side A)

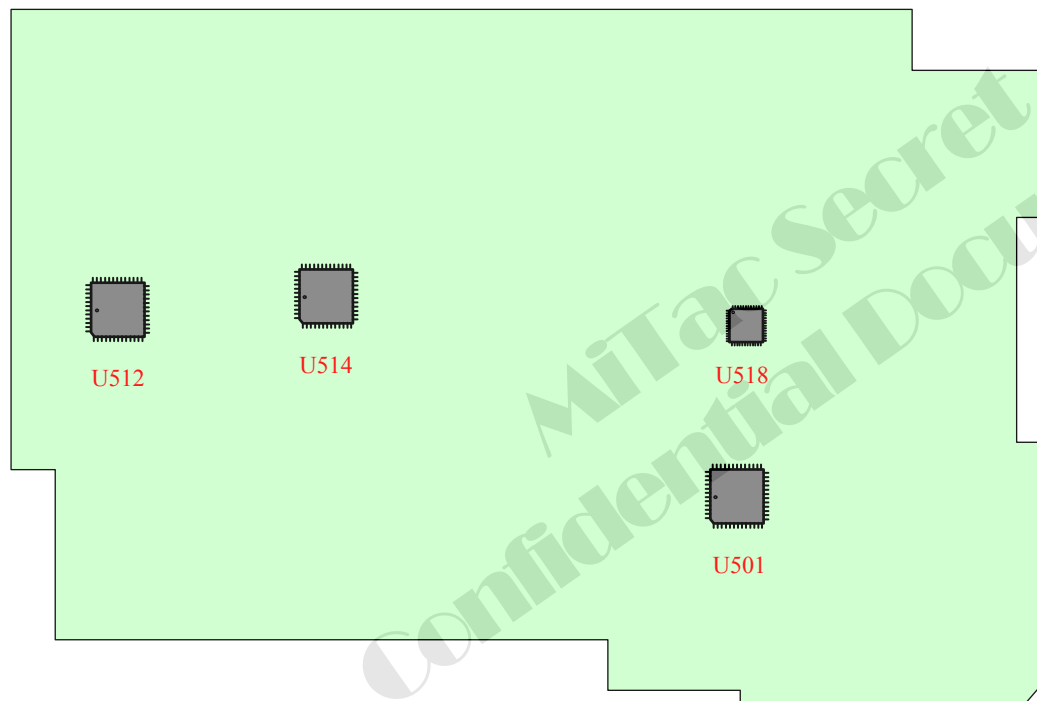


- U504 : Intel Yonah Processor
- U505 : Intel 945GM North Bridge
- U506 : Intel ICH7-M South Bridge
- U508 : System BIOS
- U509 : KBC BIOS
- U510 : Graphics Codec ATI M54

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4. Definition & Location of Major Components

4.2 I/O Board (Side B)

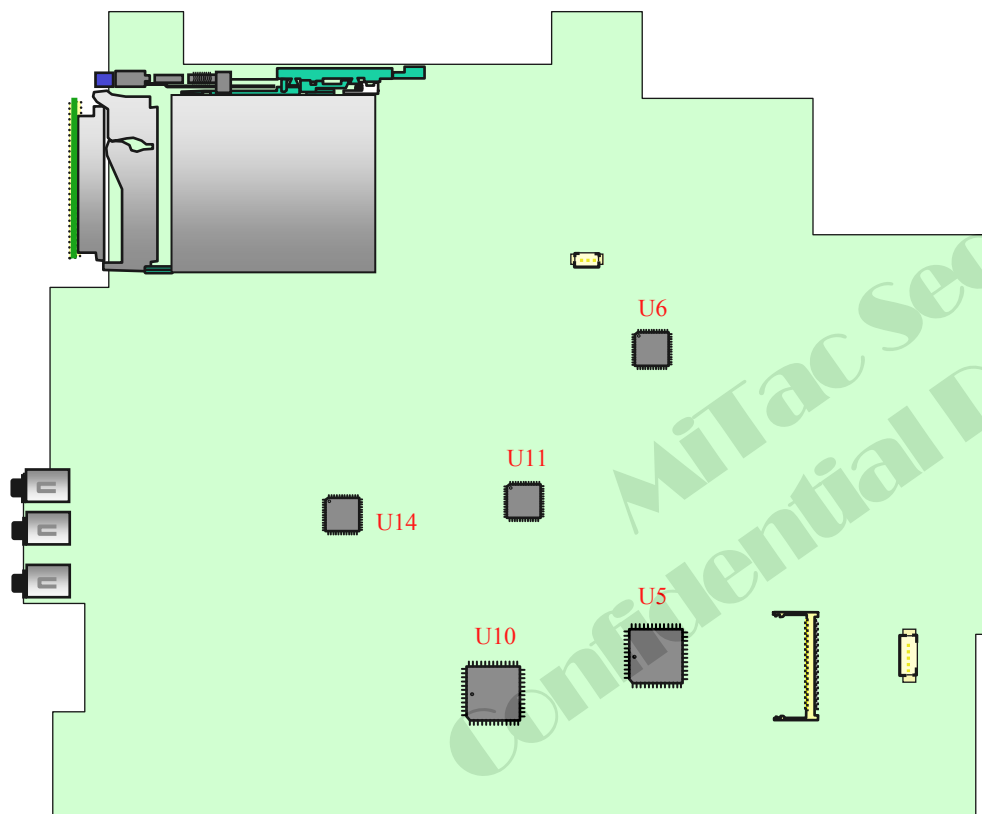


- U501 : PCI To ISA Bridge W83628F
- U509 : PCI To ISA Bridge W83628D
- U512 : LPC_ISA
- U514 : Giga Lan

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4. Definition & Location of Major Components

4.3 PCMCIA Board



- U5 : TI_PC11520PDV
- U6 : Power Matrix TPS2224A
- U10 : TI 1394B HOST TSB82AA2
- U11 : Audio codec ALC260
- U14 : Amplifier TPA0212

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5. Pin Descriptions of Major Components

5.1 Intel Yonah Processor CPU (1)

CPU Pin Description

Signal Name	Type	Description						
A[31:3]#	I/O	A[31:]#(Address) define a 2*32- byte physical memory address space. In sub-phase 1 of the address phase, these pins transmit the address of a transaction. Must connect the appropriate pins of both agents on the Intel Core TM Duo processor and the Intel Core TM Solo processor FSB. A[31:3]# are source synchronous signals and are latched into the receiving buffers by ADSTB[1:0]#. Address signals are used as straps which are sampled before RESET# is deasserted.						
A20M#	I	If A20M#(Address-20 Mask) is asserted, the processor masks physical address bit 20(A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-Mbyte boundary. Assertion of A20M# is only supported in real mode. A20M# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.						
ADS#	I/O	ADS#(Address Strobe) is asserted to indicate the validity of the transaction address on the A[31:3]# and REQ[4:0]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction.						
ADSTB#	I/O	Address strobes are used to latch A[31:3]# and REQ[4:0]# on their rising and falling edges. Strobes are associated with signals as shown below. <table><tr><th>Signals</th><th>Associated Strobe</th></tr><tr><td>REQ[4:0]#, A[16:3]#</td><td>ADSTB[0]#</td></tr><tr><td>A[31:17]#</td><td>ADSTB[1]#</td></tr></table>	Signals	Associated Strobe	REQ[4:0]#, A[16:3]#	ADSTB[0]#	A[31:17]#	ADSTB[1]#
Signals	Associated Strobe							
REQ[4:0]#, A[16:3]#	ADSTB[0]#							
A[31:17]#	ADSTB[1]#							
BCLK[1:0]	I	The differential pair BCLK (Bus Clock) determines the system bus frequency. All processor system bus agents must receive these signals to drive their outputs and latch their inputs.						
BNR#	I/O	BNR# (Block Next Request) is used to assert a bus stall by any bus agent that is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions.						

CPU Pin Description (Continued)

Signal Name	Type	Description																				
BPM[2:1]# BPM[3,0]#	I/O	BPM[3:0]# (Breakpoint Monitor) are breakpoint and performance monitor signals. They are outputs from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance. BPM[3:0]# should connect the appropriate pins of all Intel Pentium M processor system bus agents. This includes debug or performance monitoring tools.																				
BPRI#	I	BPRI# (Bus Priority Request) is used to arbitrate for ownership of the processor system bus. It must connect the appropriate pins of both processor system bus agents. Observing BPRI# active (as asserted by the priority agent) causes the other agent to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by deasserting BPRI#.																				
BR0#	I/O	BR0# is used by the processor to request the bus. The arbitration is done between the Intel Pentium M processor (Symmetric Agent) and the Mobile Intel 945 Express chipset family (High Priority Agent).																				
BSEL[2:0]	O	BSEL[2:0] (Bus SELECT) are used to select the processor input clock frequency. The table defines the possible combinations of the signals and the frequency associated with each combination. The required frequency is determined by the processor, chipset and clock synthesizer. All agents must operate at the same frequency. The processor operates at 667 MHz or 533 MHz system bus frequency (166MHz or 133MHz BCLK[1:0] frequency, respectively). BSE[2:0] Encoding for BCLK Frequency <table><tr><td>BSEL[2]</td><td>BSEL[1]</td><td>BSE[0]</td><td>BCLK Frequency</td></tr><tr><td>L</td><td>L</td><td>L</td><td>Reserved</td></tr><tr><td>L</td><td>L</td><td>H</td><td>133MHz</td></tr><tr><td>L</td><td>H</td><td>L</td><td>Reserved</td></tr><tr><td>L</td><td>H</td><td>H</td><td>166MHz</td></tr></table>	BSEL[2]	BSEL[1]	BSE[0]	BCLK Frequency	L	L	L	Reserved	L	L	H	133MHz	L	H	L	Reserved	L	H	H	166MHz
BSEL[2]	BSEL[1]	BSE[0]	BCLK Frequency																			
L	L	L	Reserved																			
L	L	H	133MHz																			
L	H	L	Reserved																			
L	H	H	166MHz																			
COMPP3:0]	Analog	COMP[3:0] must be terminated on the system board using precision (1% tolerance) resistors. Refer to the platform design guides for more implementation details.																				

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5.1 Intel Yonah Processor CPU (2)

CPU Pin Description (Continued)

Signal Name	Type	Description															
D[63:0]#	I/O	D[63:0]# (Data) are the data signals. These signals provide a 64-bit data path between the processor system bus agents, and must connect the appropriate pins on both agents. The data driver asserts DRDY# to indicate a valid data transfer. D[63:0]# are quad-pumped signals and will thus be driven four times in a common clock period. D[63:0]# are latched off the falling edge of both DSTBP[3:0]# and DSTBN[3:0]#. Each group of 16 data signals correspond to a pair of one DSTBP# and one DSTBN#. The following table shows the grouping of data signals to data strobes and DINV#. Quad-Pumped Signal Groups <table> <tr> <th>Data Group</th><th>DSTBN#/DSTBP#</th><th>DINV#</th></tr> <tr> <td>D[15:0]#</td><td>0</td><td>0</td></tr> <tr> <td>D[31:16]#</td><td>1</td><td>1</td></tr> <tr> <td>D[47:32]#</td><td>2</td><td>2</td></tr> <tr> <td>D[63:48]#</td><td>3</td><td>3</td></tr> </table> Furthermore, the DINV# pins determine the polarity of the data signals. Each group of 16 data signals corresponds to one DINV# signal. When the DINV# signal is active, the corresponding data group is inverted and therefore sampled active high.	Data Group	DSTBN#/DSTBP#	DINV#	D[15:0]#	0	0	D[31:16]#	1	1	D[47:32]#	2	2	D[63:48]#	3	3
Data Group	DSTBN#/DSTBP#	DINV#															
D[15:0]#	0	0															
D[31:16]#	1	1															
D[47:32]#	2	2															
D[63:48]#	3	3															
DBR#	O	DBR# (Data Bus Reset) is used only in processor systems where no debug port is implemented on the system board. DBR# is used by a debug port interposer so that an in-target probe can drive system reset. If a debug port is implemented in the system, DBR# is a no connect. DBR# is not a processor signal.															
DBSY#	I/O	DBSY# (Data Bus Busy) is asserted by the agent responsible for driving data on the processor system bus to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must connect the appropriate pins on both processor system bus agents.															
DEFER#	I	DEFER# is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or Input/Output agent. This signal must connect the appropriate pins of both processor system bus agents.															

CPU Pin Description (Continued)

Signal Name	Type	Description										
DINV[3:0]#	I/O	DINV[3:0]# (Data Bus Inversion) are source synchronous and indicate the polarity of the D[63:0]# signals. The DINV[3:0]# signals are activated when the data on the data bus is inverted. The bus agent will invert the data bus signals if more than half the bits, within the covered group, would change level in the next cycle. DINV[3:0]# Assignment To Data Bus <table><tr><th>Bus Signal</th><th>Data Bus Signals</th></tr><tr><td>DINV[3]#</td><td>D[63:48]#</td></tr><tr><td>DINV[2]#</td><td>D[47:32]#</td></tr><tr><td>DINV[1]#</td><td>D[31:16]#</td></tr><tr><td>DINV[0]#</td><td>D[15:0]#</td></tr></table>	Bus Signal	Data Bus Signals	DINV[3]#	D[63:48]#	DINV[2]#	D[47:32]#	DINV[1]#	D[31:16]#	DINV[0]#	D[15:0]#
Bus Signal	Data Bus Signals											
DINV[3]#	D[63:48]#											
DINV[2]#	D[47:32]#											
DINV[1]#	D[31:16]#											
DINV[0]#	D[15:0]#											
DPRSTP#	I	DPRSTP# when asserted on the platform causes the processor to transition from the Deep Sleep State to the Deeper Sleep Stated. In order to return to the Deep Sleep State, DPRSTP# must be deasserted. DPRSTP# is driven by the Intel ICH7M chipset.										
DPSLP#	I	DPSLP# when asserted on the platform causes the processor to transition from the Sleep state to the Deep Sleep state. In order to return to the Sleep state, DPSLP# must be deasserted. DPSLP# is driven by the ICH7M chipset.										
DRDY#	I/O	DRDY# (Data Ready) is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-common clock data transfer, DRDY# may be deasserted to insert idle clocks. This signal must connect the appropriate pins of both processor system bus agents.										
DSTBN[3:0]#	I/O	Data strobe used to latch in D[63:0]#. <table><tr><th>Signals</th><th>Associated Strobe</th></tr><tr><td>D[15:0]#, DINV[0]#</td><td>DSTBN[0]#</td></tr><tr><td>D[31:16]#, DINV[1]#</td><td>DSTBN[1]#</td></tr><tr><td>D[47:32]#, DINV[2]#</td><td>DSTBN[2]#</td></tr><tr><td>D[63:48]#, DINV[3]#</td><td>DSTBN[3]#</td></tr></table>	Signals	Associated Strobe	D[15:0]#, DINV[0]#	DSTBN[0]#	D[31:16]#, DINV[1]#	DSTBN[1]#	D[47:32]#, DINV[2]#	DSTBN[2]#	D[63:48]#, DINV[3]#	DSTBN[3]#
Signals	Associated Strobe											
D[15:0]#, DINV[0]#	DSTBN[0]#											
D[31:16]#, DINV[1]#	DSTBN[1]#											
D[47:32]#, DINV[2]#	DSTBN[2]#											
D[63:48]#, DINV[3]#	DSTBN[3]#											

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5.1 Intel Yonah Processor CPU (3)

CPU Pin Description (Continued)

Signal Name	Type	Description										
DSTBP[3:0]#	I/O	Data strobe used to latch in D[63:0]#.										
		<table><tr><th>Signals</th><th>Associated Strobe</th></tr><tr><td>D[15:0]#, DINV[0]#</td><td>DSTBP[0]#</td></tr><tr><td>D[31:16]#, DINV[1]#</td><td>DSTBP[1]#</td></tr><tr><td>D[47:32]#, DINV[2]#</td><td>DSTBP[2]#</td></tr><tr><td>D[63:48]#, DINV[3]#</td><td>DSTBP[3]#</td></tr></table>	Signals	Associated Strobe	D[15:0]#, DINV[0]#	DSTBP[0]#	D[31:16]#, DINV[1]#	DSTBP[1]#	D[47:32]#, DINV[2]#	DSTBP[2]#	D[63:48]#, DINV[3]#	DSTBP[3]#
		Signals	Associated Strobe									
		D[15:0]#, DINV[0]#	DSTBP[0]#									
		D[31:16]#, DINV[1]#	DSTBP[1]#									
D[47:32]#, DINV[2]#	DSTBP[2]#											
D[63:48]#, DINV[3]#	DSTBP[3]#											
FERR#/PBE#	O	FERR# (Floating-point Error)/PBE#(Pending Break Event) is a multiplexed signal and its meaning is qualified by STPCLK#. When STPCLK# is not asserted, FERR#/PBE# indicates a floating point when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel 80387 coprocessor, and is included for compatibility with systems using MS-DOS* type floating-point error reporting. When STPCLK# is asserted, an assertion of FERR#/PBE# indicates that the processor has a pending break event waiting for service. The assertion of FERR#/PBE# indicates that the processor should be returned to the Normal state. When FERR#/PBE# is asserted, indicating a break event, it will remain asserted until STPCLK# is deasserted. Assertion of PREQ# when STPCLK# is active will also cause an FERR# break event. For additional information on the pending break event functionality, including identification of support of the feature and enable/disable information, refer to Volume 3 of the Intel Architecture Software Developer's Manual and AP-485, For termination requirements please contact your Intel representative.										
GTLREF	I	GTLREF determines the signal reference level for AGTL+ input pins. GTLREF should be set at 2/3 VCCP . GTLREF is used by the AGTL+ receivers to determine if a signal is a logical 0 or logical 1.Please contact your Intel representative for more information regarding GTLREF implementation.										
HIT# HITM#	I/O I/O	HIT# (Snoop Hit) and HITM# (Hit Modified) convey transaction snoop operation results. Either system bus agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.										
IERR#	O	IERR# (Internal Error) is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the processor system bus. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#, BINIT#, or INIT#.										

CPU Pin Description (Continued)

Signal Name	Type	Description
IGNNE#	I	IGNNE# (Ignore Numeric Error) is asserted to force the processor to ignore a numeric error and continue to execute noncontrol floating-point instructions. If IGNNE# is deasserted, the processor generates an exception on a noncontrol floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 (CR0) is set. IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.
INIT#	I	INIT#(Initialization), when asserted, resets integer registers inside the processor without affecting its internal caches or floating-point registers. The processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output Write Instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction, INIT# must connect the appropriate pins of both FSB agents. If INIT# is sampled active on the active to inactive transition of RESET#, then the processor executes its Built-in Self-Test(BIST).
LINT[1:0]	I	LINT[1:0] (Local APIC Interrupt) must connect the appropriate pins of all APIC Bus agents. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium processor. Both signals are asynchronous. Both of these signals must be software configured using BIOS programming of the APIC register space and used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration.

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5.1 Intel Yonah Processor CPU (4)

CPU Pin Description (Continued)

Signal Name	Type	Description
LOCK#	I/O	LOCK# indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins of both processor system bus agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction to the end of the last transaction. When the priority agent asserts BPRI# to arbitrate for ownership of the processor system bus, it will wait until it observes LOCK# deasserted. This enables symmetric agents to retain ownership of the processor system bus throughout the bus locked operation and ensure the atomicity of lock.
PRDY#	O	Probe Ready signal used by debug tools to determine processor debug readiness.
PREQ#	I	Probe Request signal used by debug tools to request debug operation of the processor.
PROCHOT#	I/O	As an output, PROCHOT# (Processor Hot) will go active when the processor temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit has been activated, if enabled. As an input, assertion of PROCHOT# by the system will activate the TCC, if enabled. TCC will remain active until the system deasserts PROCHOT#. By default PROCHOT# is configured as an output only. Bidirectional PROCHOT# must be enabled via the BIOS. This signal may require voltage translation on the motherboard.
PSI#	O	Processor Power Status Indicator signal. This signal is asserted when the processor is in a lower state (HFM and LFM) and lower state (Deep Sleep and Deeper Sleep).
PWRGOOD	I	PWRGOOD (Power Good) is a processor input. The processor requires this signal as a clean indication that the clocks and power supplies are stable and within their specifications. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout the boundary scan operation.
REQ[4:0]	I/O	REQ[4:0]#(Request Command) must connect the appropriate pins of both FSB agents. They are asserted by the current bus owner to the currently active transaction type. These signals are source synchronous to ADSTB[0]#.

CPU Pin Description (Continued)

Signal Name	Type	Description
RESET#	I	Asserting the RESET# signal resets the processor to a known state and invalidates its internal caches without writing back any of their contents. For a power-on Reset, RESET# must stay active for at least two milliseconds after VCC and BCLK have reached their proper specifications. On observing active RESET#, both system bus agents will deassert their outputs within two clocks. All processor straps must be valid within the specified setup time before RESET# is deasserted. There is a 55 (normal) ohm die pull up resistor on this signal.
RS[2:0]#	I	RS[2:0]# (Response Status) are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of both processor system bus agents.
RSVD	Reserved/ No Connect	These pins are RESERVED and must be left unconnected on the board. However, it is recommended that routing channels to these pins on the board be kept open for possible future use. Please refer to the platform design guides for more details.
SLP#	I	SLP# (Sleep), when asserted in Stop-Grant state, causes the processor to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. The processor will recognize only assertion of the RESET# signal, deassertion of SLP#, and removal of the BCLK input while in Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and processor core units. If DPSLP# is asserted while in the Sleep state, the processor will exit the Sleep state and transition to the Deep Sleep state.
SMI#	I	SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enter System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler. If SMI# is asserted during the deassertion of RESET# the processor will tristate its outputs.

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5.1 Intel Yonah Processor CPU (5)

CPU Pin Description (Continued)

Signal Name	Type	Description
STPCLK#	I	STPCLK# (Stop Clock), when asserted, causes the processor to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the system bus and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.
TCK	I	TCK (Test Clock) provides the clock input for the processor Test Bus (also known as the Test Access Port).
TDI	I	TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.
TDO	O	TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.
TEST1,	I	TEST1 must have a stuffing option of separate pull down resistor to Vss.
TEST2	I	TEST2 must have a 51±5% pull down resistor to Vss.
THERMDA	Other	Thermal Diode Anode.
THERMDC	Other	Thermal Diode Cathode.
THERMTRIP#	O	The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all execution when the junction temperature exceeds approximately 125°C. This is signalled to the system by the THERMTRIP# (Thermal Trip) pin.
TMS	I	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.
TRDY#	I	TRDY# (Target Ready) is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of both FSB agents.
TRST#	I	TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset.
Vcc	I	Processor core power supply.
Vcca	I	Vcca provides isolated power for the internal processor core PLL's.
Vccp	I	Processor I/O Power Supply.

CPU Pin Description (Continued)

Signal Name	Type	Description
VID[6:0]	O	VID[6:0] (Voltage ID) pins are used to support automatic selection of power supply voltages (Vcc). Unlike some previous generations of processors, these are CMOS signals that are driven by the Intel Pentium M processor. The voltage supply for these pins must be valid before the VR can supply Vcc to the processor. Conversely, the VR output must be disabled until the voltage supply for the VID pins becomes valid. The VID pins are needed to support the processor voltage specification variations. The VR must supply the voltage that is requested by the pins, or disable itself.
Vssense	O	Vssense together with Vccsense are voltage feedback signals to IMVP6 that control the 2.1m loadline at the processor die. It should be used to sense ground near the silicon with little noise.

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5.2 Intel 945GM North Bridge (1)

Host Interface Signals

Signal Name	Type	Description
HADS#	I/O GTL+	Address Strobe: The processor bus owner asserts HADS# to indicate the first of two cycles of a request phase. The (G)MCH can assert this signal for snoop cycles and interrupt messages.
HBNR#	I/O GTL+	Block Next Request: HBNR# is used to block the current request bus owner from issuing new requests. This signal is used to dynamically control the processor bus pipeline depth.
HPRI#	O GTL+	Priority Agent Bus Request: The (G)MCH is the only Priority Agent on the processor bus. It asserts this signal to obtain the ownership of the address bus. This signal has priority over symmetric bus requests and will cause the current symmetric owner to stop issuing new transactions unless the HLOCK# signal was asserted.
HBREQ0#	I/O GTL+	Bus Request 0: The (G)MCH pulls the processor's bus HBREQ0# signal low during HCPURST#. The processor samples this signal on the active-toinactive transition of HCPURST#. The minimum setup time for this signal is 4 HCLKs. The minimum hold time is 2 HCLKs and the maximum hold time is 20 HCLKs. HBREQ0# should be tristated after the hold time requirement has been satisfied.
HCPURST#	O GTL+	CPU Reset: The HCPURST# pin is an output from the (G)MCH. The (G)MCH asserts HCPURST# while RSTIN# is asserted and for approximately 1 ms after RSTIN# is de-asserted. The HCPURST# allows the processors to begin execution in a known state. Note that the Intel® ICH7 must provide processor frequency select strap setup and hold times around HCPURST#. This requires strict synchronization between (G)MCH HCPURST# de-assertion and the ICH7 driving the straps.
HDBSY#	I/O GTL+	Data Bus Busy: This signal is used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
HDEFER#	O GTL+	Defer: HDEFER# indicates that the (G)MCH will terminate the transaction currently being snooped with either a deferred response or with a retry response.

Host Interface Signals (Continued)

Signal Name	Type	Description										
HDRDY#	I/O GTL+	Data Ready: This signal is asserted for each cycle that data is transferred.										
HEDRDY#	O GTL+	Early Data Ready: This signal indicates that the data phase of a read transaction will start on the bus exactly one common clock after assertion.										
HDINV[3:0]#	I/O GTL+	Dynamic Bus Inversion: These signals are driven along with the HD[63:0] signals. They indicate if the associated signals are inverted or not. HDINV[3:0]# are asserted such that the number of data bits driven electrically low (low voltage) within the corresponding 16 bit group never exceeds 8.. <table><tr><td>HDINV[x]#</td><td>Data Bits</td></tr><tr><td>HDINV3#</td><td>HD[63:48]</td></tr><tr><td>HDINV2#</td><td>HD[47:32]</td></tr><tr><td>HDINV1#</td><td>HD[31:16]</td></tr><tr><td>HDINV0#</td><td>HD[15:0]</td></tr></table>	HDINV[x]#	Data Bits	HDINV3#	HD[63:48]	HDINV2#	HD[47:32]	HDINV1#	HD[31:16]	HDINV0#	HD[15:0]
HDINV[x]#	Data Bits											
HDINV3#	HD[63:48]											
HDINV2#	HD[47:32]											
HDINV1#	HD[31:16]											
HDINV0#	HD[15:0]											
HA[31:3]#	I/O GTL+	Host Address Bus: HA[31:3]# connect to the processor address bus. During processor cycles, the HA[31:3]# are inputs. The (G)MCH drives HA[31:3]# during snoop cycles on behalf of DMI and PCI Express* initiators. HA[31:3]# are transferred at 2x rate.										
HADSTB[1:0]#	I/O GTL+	Host Address Strobe: These signals are the source synchronous strobes used to transfer HA[31:3]# and HREQ[4:0] at the 2x transfer rate.										
HD[63:0]#	I/O GTL+	Host Data: These signals are connected to the processor data bus. Data on HD[63:0] is transferred at 4x rate. Note that the data signals may be inverted on the processor bus, depending on the HDINV[3:0]# signals.										
HHIT#	I/O GTL+	Hit: This signal indicates that a caching agent holds an unmodified version of the requested line. In addition, HHIT# is driven in conjunction with HHITM# by the target to extend the snoop window.										

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5.2 Intel 945GM North Bridge (2)

Host Interface Signals (Continued)

Signal Name	Type	Description															
HDSTBP[3:0]# HDSTBN[3:0]#	I/O GTL+	Differential Host Data Strobes: These signals are the differential source synchronous strobes used to transfer HD[63:0]# and HDINV[3:0]# at 4x transfer rate. These signals are named this way because they are not level sensitive. Data is captured on the falling edge of both strobes. Hence they are pseudo-differential, and not true differential. <table> <tr> <th>Strobe</th><th>Data</th><th>Bits</th></tr> <tr> <td>HDSTBP3#, HDSTBN3#</td><td>HD[63:48]</td><td>HDINV3#</td></tr> <tr> <td>HDSTBP2#, HDSTBN2#</td><td>HD[47:32]</td><td>HDINV2#</td></tr> <tr> <td>HDSTBP1#, HDSTBN1#</td><td>HD[31:16]</td><td>HDINV1#</td></tr> <tr> <td>HDSTBP0#, HDSTBN0#</td><td>HD[15:00]</td><td>HDINV0#</td></tr> </table>	Strobe	Data	Bits	HDSTBP3#, HDSTBN3#	HD[63:48]	HDINV3#	HDSTBP2#, HDSTBN2#	HD[47:32]	HDINV2#	HDSTBP1#, HDSTBN1#	HD[31:16]	HDINV1#	HDSTBP0#, HDSTBN0#	HD[15:00]	HDINV0#
Strobe	Data	Bits															
HDSTBP3#, HDSTBN3#	HD[63:48]	HDINV3#															
HDSTBP2#, HDSTBN2#	HD[47:32]	HDINV2#															
HDSTBP1#, HDSTBN1#	HD[31:16]	HDINV1#															
HDSTBP0#, HDSTBN0#	HD[15:00]	HDINV0#															
HHITM#	I/O GTL+	Hit Modified: This signal indicates that a caching agent holds a modified version of the requested line and that this agent assumes responsibility for providing the line. In addition, HHITM# is driven in conjunction with HHIT# to extend the snoop window.															
HLOCK#	I/O GTL+	Host Lock: All processor bus cycles sampled with the assertion of HLOCK# and HADS#, until the negation of HLOCK# must be atomic (i.e., no DMI or PCI Express accesses to DRAM are allowed when HLOCK# is asserted by the processor).															
HPCREQ#	I GTL+ 2X	Precharge Request: The processor provides a "hint" to the (G)MCH that it is OK to close the DRAM page of the memory read request with which the hint is associated. The (G)MCH uses this information to schedule the read request to memory using the special "AutoPrecharge" attribute. This causes the DRAM to immediately close (Precharge) the page after the read data has been returned. This allows subsequent processor requests to more quickly access information on other DRAM pages, since it will no longer be necessary to close an open page prior to opening the proper page. HPCREQ# is asserted by the requesting agent during both halves of Request Phase. The same information is provided in both halves of the request phase.															
HREQ[4:0]#	I/O GTL+ 2X	Host Request Command: These signals define the attributes of the request. HREQ[4:0]# are transferred at 2x rate. They are asserted by the requesting agent during both halves of Request Phase. In the first half, the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second half, the signals carry additional information to define the complete transaction type.															

Host Interface Signals (Continued)

Signal Name	Type	Description
HTRDY#	O GTL+	Host Target Ready: This signal indicates that the target of the processor transaction is able to enter the data transfer phase.
HRS[2:0]#	O GTL+	Host Response Status: These signals indicate the type of response as shown below: 000 = Idle state 001 = Retry response 010 = Deferred response 011 = Reserved (not driven by (G)MCH) 100 = Hard Failure (not driven by (G)MCH) 101 = No data response 110 = Implicit Write back 111 = Normal data response
BSEL[2:0]	I COMS	Bus Speed Select: At the de-assertion of RSTIN#, the value sampled on these pins determines the expected frequency of the bus.
HRCOMP	I/O COMS	Host RCOMP: This signal is used to calibrate the Host GTL+ I/O buffers. This signal is powered by the Host Interface termination rail (V _{TT}).
HSCOMP	I/O COMS	Slew Rate Compensation: This is the compensation signal for the Host Interface.
HSWING	I A	Host Voltage Swing: This signal provides the reference voltage used by FSB RCOMP circuits. HSWING is used for the signals handled by HRCOMP.
HDVREF	I A	Host Reference Voltage: Voltage input for the data, address, and common clock signals of the Host GTL interface.
HACCVREF	I A	Host Reference Voltage: Reference voltage input for the Address, and Common clock signals of the Host GTL interface.

Note: Unless otherwise noted, the voltage level for all signals in this interface is tied to the termination voltage of the Host Bus (V_{TT}).

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5.2 Intel 945GM North Bridge (3)

DDR2 DRAM Channel A Interface

Signal Name	Type	Description
SCLK_A[5:0]	O SSTL-1.8	SDRAM Differential Clock: (3 per DIMM). SCLK_Ax and its complement SCLK_Ax# signal make a differential clock pair output. The crossing of the positive edge of SCLK_Ax and the negative edge of its complement SCLK_Ax# are used to sample the command and control signals on the SDRAM.
SCLK_A[5:0]#	O SSTL-1.8	SDRAM Complementary Differential Clock: (3 per DIMM). These are the complementary Differential DDR2 Clock signals.
SCS_A[3:0]#	O SSTL-1.8	Chip Select: (1 per Rank). These signals select particular SDRAM components during the active state. There is one chip select for each SDRAM rank.
SMA_A[13:0]	O SSTL-1.8	Memory Address: These signals are used to provide the multiplexed row and column address to the SDRAM.
SBS_A[2:0]	O SSTL-1.8	Bank Select: These signals define which banks are selected within each SDRAM rank. DDR2: 1-Gb technology is 8 banks.
SRAS_A#	O SSTL-1.8	Row Address Strobe: This signal is used with SCAS_A# and SWE_A# (along with SCS_A#) to define the SDRAM commands.
SCAS_A#	O SSTL-1.8	Column Address Strobe: This signal is used with SRAS_A# and SWE_A# (along with SCS_A#) to define the SDRAM commands.
SWE_A#	O SSTL-1.8	Write Enable: This signal is used with SCAS_A# and SRAS_A# (along with SCS_A#) to define the SDRAM commands.
SDQ_A[63:0]	I/O SSTL-1.8 2X	Data Lines: The SDQ_A[63:0] signals interface to the SDRAM data bus.
SDM_A[7:0]	O SSTL-1.8 2X	Data Mask: When activated during writes, the corresponding data groups in the SDRAM are masked. There is one SDM_Ax bit for every data byte lane.
SDQS_A[7:0]	I/O SSTL-1.8 2X	Data Strobes: For DDR2, SDQS_Ax and its complement SDQS_Ax# signal make up a differential strobe pair. The data is captured at the crossing point of SDQS_Ax and its complement SDQS_Ax# during read and write transactions.

DDR2 DRAM Channel A Interface (Continued)

Signal Name	Type	Description
SDQS_A[7:0]#	I/O SSTL-1.8 2X	Data Strobe Complements: These are the complementary DDR2 strobe signals.
SCKE_A[3:0]	O SSTL-1.8	Clock Enable: (1 per Rank). SCKE_Ax is used to initialize the SDRAMs during power-up, to power-down SDRAM ranks, and to place all SDRAM ranks into and out of self-refresh during Suspend-to-RAM.
SODT_A[3:0]	O SSTL-1.8	On Die Termination: Active On-die Termination Control signals for DDR2 devices.

DDR2 DRAM Channel B Interface

Signal Name	Type	Description
SCLK_B[5:0]	O SSTL-1.8	SDRAM Differential Clock: (3 per DIMM). SCLK_Bx and its complement SCLK_Bx# signal make a differential clock pair output. The crossing of the positive edge of SCLK_Bx and the negative edge of its complement SCLK_Bx# are used to sample the command and control signals on the SDRAM.
SCLK_B[5:0]#	O SSTL-1.8	SDRAM Complementary Differential Clock: (3 per DIMM). These are the complementary Differential DDR2 Clock signals.
SCS_B[3:0]#	O SSTL-1.8	Chip Select: (1 per Rank). These signals select particular SDRAM components during the active state. There is one chip select for each SDRAM rank.
SMA_B[13:0]	O SSTL-1.8	Memory Address: These signals are used to provide the multiplexed row and column address to the SDRAM.
SBS_B[2:0]	O SSTL-1.8	Bank Select: These signals define which banks are selected within each SDRAM rank. DDR2: 1-Gb technology is 8 banks.
SRAS_B#	O SSTL-1.8	Row Address Strobe: This signal is used with SCAS_B# and SWE_B# (along with SCS_B#) to define the SDRAM commands.

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5.2 Intel 945GM North Bridge (4)

DDR2 DRAM Channel B Interface (Continued)

Signal Name	Type	Description
SCAS_B#	O SSTL-1.8	Column Address Strobe: This signal is used with SRAS_B# and SWE_B# (along with SCS_B#) to define the SDRAM commands.
SWE_B#	O SSTL-1.8	Write Enable: This signal is used with SCAS_B# and SRAS_B# (along with SCS_B#) to define the SDRAM commands.
SDQ_B[63:0]	I/O SSTL-1.8 2X	Data Lines: The SDQ_B[63:0] signals interface to the SDRAM data bus.
SDM_B[7:0]	O SSTL-1.8 2X	Data Mask: When activated during writes, the corresponding data groups in the SDRAM are masked. There is one SDM_Bx bit for every data byte lane.
SDQS_B[7:0]	I/O SSTL-1.8 2X	Data Strobes: For DDR2, SDQS_Bx and its complement SDQS_Bx# signal make up a differential strobe pair. The data is captured at the crossing point of SDQS_Bx and its complement SDQS_Bx# during read and write transactions.
SDQS_B[7:0]#	I/O SSTL-1.8 2X	Data Strobe Complements: These are the complementary DDR2 strobe signals.
SCKE_B[3:0]	O SSTL-1.8	Clock Enable: (1 per Rank). SCKE_Bx is used to initialize the SDRAMs during power-up, to power-down SDRAM ranks, and to place all SDRAM ranks into and out of self-refresh during Suspend-to-RAM.
SODT_B[3:0]	O SSTL-1.8	On Die Termination: Active On-die Termination Control signals for DDR2 devices.

PCI Express* Interface Signals

Signal Name	Type	Description
EXP_RXN[15:0] EXP_RXP[15:0]	I/O PCIE	PCI Express* Receive Differential Pair
EXP_TXN[15:0] EXP_TXP[15:0]	O PCIE	PCI Express* Transmit Differential Pair
EXP_ICOMPO	I A	PCI Express* Output Current and Resistance Compensation
EXP_COMPI	I A	PCI Express* Input Current Compensation

Unless otherwise specified, PCI Express signals are AC coupled, so the only voltage specified is a maximum 1.2 V differential swing.

Analog Display Signals (Intel® 82945G GMCH Only)

Signal Name	Type	Description
RED	O A	RED Analog Video Output: This signal is a CRT Analog video output from the internal color palette DAC. The DAC is designed for a 37.5 Ω routing impedance; however, the terminating resistor to ground will be 75 Ω (e.g., 75 Ω resistor on the board, in parallel with a 75 Ω CRT load).
RED#	O A	REDB Analog Output: This signal is an analog video output from the internal color palette DAC. It should be shorted to the ground plane.
GREEN	O A	GREEN Analog Video Output: This signal is a CRT Analog video output from the internal color palette DAC. The DAC is designed for a 37.5 Ω routing impedance; however, the terminating resistor to ground will be 75 Ω (e.g., 75 Ω resistor on the board, in parallel with a 75 Ω CRT load).
GREEN#	O A	GREENB Analog Output: This signal is an analog video output from the internal color palette DAC. It should be shorted to the ground plane.
BLUE	O A	BLUE Analog Video Output: This signal is a CRT Analog video output from the internal color palette DAC. The DAC is designed for a 37.5 Ω routing impedance; however, the terminating resistor to ground will be 75 Ω (e.g., 75 Ω resistor on the board, in parallel with a 75 Ω CRT load).
BLUE#	O A	BLUEB Analog Output: This signal is an analog video output from the internal color palette DAC. It should be shorted to the ground plane.
REFSET	O A	Resistor Set: Set point resistor for the internal color palette DAC. A 255 Ω 1% resistor is required between REFSET and motherboard ground.
HSYNC	O 2.5V CMOS	CRT Horizontal Synchronization: This signal is used as the horizontal sync (polarity is programmable) or "sync interval". 2.5 V output.
VSYNC	O 2.5V CMOS	CRT Vertical Synchronization: This signal is used as the vertical sync (polarity is programmable). 2.5 V output.
DDC_CLK	I/O 2.5V CMOS	Monitor Control Clock: This signal may be used as the DDC_CLK for a secondary multiplexed digital display connector.
DDC_DATA	I/O 2.5V CMOS	Monitor Control Data: This signal may be used as the DDC_Data for a secondary multiplexed digital display connector.

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5.2 Intel 945GM North Bridge (5)

Clock, Reset, and Miscellaneous

Signal Name	Type	Description
HCLKP HCLKN	I HCSL	Differential Host Clock In: These pins receive a differential host clock from the external clock synthesizer. This clock is used by all of the (G)MCH logic that is in the Host clock domain. Memory domain clocks are also derived from this source.
GCLKP GCLKN	I HCSL	Differential PCI Express* Clock In: These pins receive a differential 100 MHz Serial Reference clock from the external clock synthesizer. This clock is used to generate the clocks necessary for the support of PCI Express.
DREFCLKN DREFCLKP	I HCSL	Display PLL Differential Clock In
RSTIN#	I HVIN	Reset In: When asserted, this signal will asynchronously reset the (G)MCH logic. This signal is connected to the PCIRST# output of the Intel® ICH7. All PCI Express graphics attach output signals will also tri-state compliant to <i>PCI Express* Specification, Revision 1.0a</i> . This input should have a Schmitt trigger to avoid spurious resets. This signal is required to be 3.3 V tolerant.
PWROK	I HVIN	Power OK: When asserted, PWROK is an indication to the (G)MCH that core power has been stable for at least 10 us.
EXTTS#	I CMOS	External Thermal Sensor Input: This signal may connect to a precision thermal sensor located on or near the DIMMs. If the system temperature reaches a dangerously high value, then this signal can be used to trigger the start of system thermal management. This signal is activated when an increase in temperature causes a voltage to cross some threshold in the sensor.
EXP_EN	I CMOS	PCI Express SDVO Concurrent Select: 0 = Only SDVO or PCI Express operational 1 = SDVO and PCI Express operating simultaneously via PCI Express port NOTES: For the 82945P MCH, this signal should be pulled low.
EXP_SLR	I CMOS	PCI Express* Lane Reversal/Form Factor Selection: (G)MCH's PCI Express lane numbers are reversed to differentiate Balanced Technology Extended (BTX) or ATX form factors. 0 = (G)MCH's PCI Express lane numbers are reversed (BTX Platforms) 1 = Normal operation (ATX Platforms)
ICH_SYNC#	O HVC MOS	ICH Sync: This signal is connected to the MCH_SYNC# signal on the ICH7.

Clock, Reset, and Miscellaneous (Continued)

Signal Name	Type	Description
XORTEST	I/O GTL+	XOR Test: This signal is used for Bed of Nails testing by OEMs to execute XOR Chain test.
LLLZTEST	I/O GTL+	All Z Test: As an input this signal is used for Bed of Nails testing by OEMs to execute XOR Chain test. It is used as an output for XOR chain testing.

DDR2 DRAM Reference and Compensation

Signal Name	Type	Description
SRCOMP[1:0]	I/O	System Memory RCOMP
SOCOMP[1:0]	I/O A	DDR2 On-Die DRAM Over Current Detection (OCD) Driver Compensation
SMVREF[1:0]	I A	SDRAM Reference Voltage: These signals are reference voltage inputs for each SDQ_x, SDM_x, SDQS_x, and SDQS_x# input signals.

Direct Media Interface (DMI)

Signal Name	Type	Description
DMI_RXP[3:0] DMI_RXN[3:0]	I/O DMI	Direct Media Interface: These signals are receive differential pairs (Rx).
DMI_TXP[3:0] DMI_TXN[3:0]	O DMI	Direct Media Interface: These signals are transmit differential pairs (Tx).

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5.2 Intel 945GM North Bridge (6)

Intel® Serial DVO (SDVO) Interface (Intel® 82945G GMCH Only)

Signal Name	Type	Description
SDVOB_CLK-	O PCIE	Serial Digital Video Channel B Clock Complement: This signal is multiplexed with EXP TXN12.
SDVOB_CLK+	O PCIE	Serial Digital Video Channel B Clock Clock: This signal is multiplexed with EXP TXP12.
SDVOB_RED-	O PCIE	Serial Digital Video Channel C Red Complement: This signal is multiplexed with EXP TXN15.
SDVOB_RED+	O PCIE	Serial Digital Video Channel C Red: This signal is multiplexed with EXP TXP15.
SDVOB_GREEN-	O PCIE	Serial Digital Video Channel B Green Complement: This signal is multiplexed with EXP TXN14.
SDVOB_GREEN+	O PCIE	Serial Digital Video Channel B Green: This signal is multiplexed with EXP TXP14.
SDVOB_BLUE-	O PCIE	Serial Digital Video Channel B Blue Complement: This signal is multiplexed with EXP TXN13.
SDVOB_BLUE+	O PCIE	Serial Digital Video Channel B Blue: This signal is multiplexed with EXP TXP13.
SDVOC_RED-/SDVOB_ALPHA-	O PCIE	Serial Digital Video Channel C Red Complement Channel B Alpha Complement: This signal is multiplexed with EXP TXN11.
SDVOC_RED+/SDVOB_ALPHA+	O PCIE	Serial Digital Video Channel C Red Complement Channel B Alpha: This signal is multiplexed with EXP TXP11.
SDVOC_GREEN-	O PCIE	Serial Digital Video Channel C Green Complement: This signal is multiplexed with EXP TXN10.
SDVOC_GREEN+	O PCIE	Serial Digital Video Channel C Green: This signal is multiplexed with EXP TXP10.
SDVOC_BLUE-	O PCIE	Serial Digital Video Channel C Blue Complement: This signal is multiplexed with EXP TXN9.
SDVOC_BLUE+	O PCIE	Serial Digital Video Channel C Blue: This signal is multiplexed with EXP TXP9.
SDVOC_CLK-	O PCIE	Serial Digital Video Channel C Clock Complement: This signal is multiplexed with EXP TXN8.
SDVOC_CLK+	O PCIE	Serial Digital Video Channel C Clock: This signal is multiplexed with EXP TXP8.
SDVO_TVCLKIN-	I PCIE	Serial Digital Video TV-OUT Synchronization Clock Complement: This signal is multiplexed with EXP RXN15.
SDVO_TVCLKIN+	I PCIE	Serial Digital Video TV-OUT Synchronization Clock: This signal is multiplexed with EXP RXP15.
SDVOB_INT-	I PCIE	Serial Digital Video Input Interrupt Complement: This signal is multiplexed with EXP RXN14.

Intel® Serial DVO (SDVO) Interface (Intel® 82945G GMCH Only) (Continued)

Signal Name	Voltage	Description
SDVOB_INT+	I PCIE	Serial Digital Video Input Interrupt: This signal is multiplexed with EXP RXP14.
SDVOC_INT-	I PCIE	Serial Digital Video Input Interrupt Complement: This signal is multiplexed with EXP RXN10.
SDVOC_INT+	I PCIE	Serial Digital Video Input Interrupt: This signal is multiplexed with EXP RXP10.
SDVO_STALL-	I PCIE	Serial Digital Video Filed Stall Complement: This signal is multiplexed with EXP RXN13.
SDVO_STALL+	I PCIE	Serial Digital Video Filed Stall: This signal is multiplexed with EXP RXP13.
SDVO_CTRLCLK	I/O COD	Serial Digital Video Device Control Clock.
SDVO_CTRLDATA	I/O COD	Serial Digital Video Device Control Data.

Power and Ground

Name	Voltage	Description
VCC	1.5V	Core Power
VTT	1.2V	Processor System Bus Power
VCC_EXP	1.5V	PCI Express* and DMI Power
VCCSM	1.8V	System Memory Power
VCC2	2.5V	2.5V COMS Power
VCCA_EXPPLL	1.5V	PCI Express PLL Analog Power
VCCA_DPLLA (GMCH ONLY)	1.5V	Display PLL A Analog Power
VCCA_DPLLB (GMCH ONLY)	1.5V	Display PLL B Analog Power
VCCA_HPLL	1.5V	Host PLL Analog Power
VCCA_SMPLL	1.5V	System Memory PLL Analog Power
VCCA_DAC	2.5V	Display DAC Analog Power
VSS	0V	Ground
VSSA_DAC	0V	Ground

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5.3 Intel ICH7-M South Bridge (1)

PCI Interface Signals

Signal Name	Type	Description
IRDY#	I/O	Initiator Ready: IRDY# indicates the ICH7's ability, as an initiator, to complete the current data phase of the transaction. It is used in conjunction with TRDY#. A data phase is completed on any clock both IRDY# and TRDY# are sampled asserted. During a write, IRDY# indicates the ICH7 has valid data present on AD[31:0]. During a read, it indicates the ICH7 is prepared to latch data. IRDY# is an input to the ICH7 when the ICH7 is the target and an output from the ICH7 when the ICH7 is an initiator. IRDY# remains tri-stated by the ICH7 until driven by an initiator.
TRDY#	I/O	Target Ready: TRDY# indicates the Intel® ICH7's ability as a target to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed when both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that the ICH7, as a target, has placed valid data on AD[31:0]. During a write, TRDY# indicates the ICH7, as a target is prepared to latch data. TRDY# is an input to the ICH7 when the ICH7 is the initiator and an output from the ICH7 when the ICH7 is a target. TRDY# is tri-stated from the leading edge of PLTRST#. TRDY# remains tri-stated by the ICH7 until driven by a target.
STOP#	I/O	Stop: STOP# indicates that the ICH7, as a target, is requesting the initiator to stop the current transaction. STOP# causes the ICH7, as an initiator, to stop the current transaction. STOP# is an output when the ICH7 is a target and an input when the ICH7 is an initiator.
PAR	I/O	Calculated/Checked Parity: PAR uses "even" parity calculated on 36 bits, AD[31:0] plus C/BE[3:0]#. "Even" parity means that the ICH7 counts the number of one within the 36 bits plus PAR and the sum is always even. The ICH7 always calculates PAR on 36 bits regardless of the valid byte enables. The ICH7 generates PAR for address and data phases and only guarantees PAR to be valid one PCI clock after the corresponding address or data phase. The ICH7 drives and tristates PAR identically to the AD[31:0] lines except that the ICH7 delays PAR by exactly one PCI clock. PAR is an output during the address phase (delayed one clock) for all ICH7 initiated transactions. PAR is an output during the data phase (delayed one clock) when the ICH7 is the initiator of a PCI write transaction, and when it is the target of a read transaction. ICH7 checks parity when it is the target of a PCI write transaction. If a parity error is detected, the ICH7 will set the appropriate internal status bits, and has the option to generate an NMI# or SMI#.

PCI Interface Signals (Continued)

Name	Type	Description
AD[31:0]	I/O	PCI Address/Data: AD[31:0] is a multiplexed address and data bus. During the first clock of a transaction, AD[31:0] contain a physical address (32 bits). During subsequent clocks, AD[31:0] contain data. The Intel® ICH7 will drive all 0s on AD[31:0] during the address phase of all PCI Special Cycles.
C/BE[3:0]#	I/O	Bus Command and Byte Enables: The command and byte enable signals are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE[3:0]# define the bus command. During the data phase C/BE[3:0]# define the Byte Enables. C/BE[3:0]# Command Type 0000b Interrupt Acknowledge 0001b Special Cycle 0010b I/O Read 0011b I/O Write 0110b Memory Read 0111b Memory Write 1010b Configuration Read 1011b Configuration Write 1100b Memory Read Multiple 1110b Memory Read Line 1111b Memory Write and Invalidate All command encodings not shown are reserved. The ICH7 does not decode reserved values, and therefore will not respond if a PCI master generates a cycle using one of the reserved values.
DEVSEL#	I/O	Device Select: The ICH7 asserts DEVSEL# to claim a PCI transaction. As an output, the ICH7 asserts DEVSEL# when a PCI master peripheral attempts an access to an internal ICH7 address or an address destined DMI (main memory or graphics). As an input, DEVSEL# indicates the response to an ICH7-initiated transaction on the PCI bus. DEVSEL# is tri-stated from the leading edge of PLTRST#. DEVSEL# remains tri-stated by the ICH7 until driven by a target device.
FRAME#	I/O	Cycle Frame: The current initiator drives FRAME# to indicate the beginning and duration of a PCI transaction. While the initiator asserts FRAME#, data transfers continue. When the initiator negates FRAME#, the transaction is in the final data phase. FRAME# is an input to the ICH7 when the ICH7 is the target, and FRAME# is an output from the ICH7 when the ICH7 is the initiator. FRAME# remains tristated by the ICH7 until driven by an initiator.

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5.3 Intel ICH7-M South Bridge (2)

PCI Interface Signals (Continued)

Signal Name	Type	Description
PERR#	I/O	Parity Error: An external PCI device drives PERR# when it receives data that has a parity error. The ICH7 drives PERR# when it detects a parity error. The ICH7 can either generate an NMI# or SMI# upon detecting a parity error (either detected internally or reported via the PERR# signal).
REQ[0:3]# REQ[4]#/ GPIO22 REQ[5]#/GPIO1	I	PCI Requests: The ICH7 supports up to 6 masters on the PCI bus. The REQ[4]# and REQ5# pins can instead be used as a GPIO.
GNT[0:3]# GNT[4]#/ GPIO48 GNT[5]#/ GPIO17#	O	PCI Grants: The ICH7 supports up to 6 masters on the PCI bus. The GNT4# and GNT5# pins can instead be used as a GPIO. Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3 power rail. GNT5#/GPIO17 has an internal pull-up.
PCICLK	I	NOTE: PCI Clock: This is a 33 MHz clock. PCICLK provides timing for all transactions on the PCI Bus.
PCIRST#	O	PCI Reset: This is the Secondary PCI Bus reset signal. It is a logical OR of the primary interface PLTRST# signal and the state of the Secondary Bus Reset bit of the Bridge Control register (D30:F0:3Eh, bit 6).
PLOCK#	I/O	PCI Lock: This signal indicates an exclusive bus operation and may require multiple transactions to complete. The ICH7 asserts PLOCK# when it performs non-exclusive transactions on the PCI bus. PLOCK# is ignored when PCI masters are granted the bus in desktop configurations.
SERR#	I/OD	System Error: SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, the ICH7 has the ability to generate an NMI, SMI#, or interrupt.
PME#	I/OD	PCI Power Management Event: PCI peripherals drive PME# to wake the system from low-power states S1–S5. PME# assertion can also be enabled to generate an SCI from the S0 state. In some cases the ICH7 may drive PME# active due to an internal wake event. The ICH7 will not drive PME# high, but it will be pulled up to VccSus3_3 by an internal pull-up resistor.

Serial ATA Interface Signals

Name	Type	Description
SATA0TXP SATA0TXN	O	Serial ATA 0 Differential Transmit Pair: These are outbound high-speed differential signals to Port 0.
SATA0RXP SATA0RXN	I	Serial ATA 0 Differential Receive Pair: These are inbound high-speed differential signals from Port 0.
SATA1TXP SATA1TXN	O	Serial ATA 1 Differential Transmit Pair: These are outbound high-speed differential signals to Port 1.
SATA1RXP SATA1RXN	I	Serial ATA 1 Differential Receive Pair: These are inbound high-speed differential signals from Port 1.
SATA2TXP SATA2TXN	O	Serial ATA 2 Differential Transmit Pair: These are outbound high-speed differential signals to Port 2.
SATA2RXP SATA2RXN	I	Serial ATA 2 Differential Receive Pair: These are inbound high-speed differential signals from Port 2.
SATA3TXP SATA3TXN	O	Serial ATA 3 Differential Transmit Pair: These are outbound high-speed differential signals to Port 3.
SATA3RXP SATA3RXN	I	Serial ATA 3 Differential Receive Pair: These are inbound high-speed differential signals from Port 3.
SATARBIAS	O	Serial ATA Resistor Bias: These are analog connection points for an external resistor to ground.
SATARBIAS#	I	Serial ATA Resistor Bias Complement: These are analog connection points for an external resistor to ground.
SATA0GP/ GPIO21	I	Serial ATA 0 General Purpose: This is an input pin which can be configured as an interlock switch corresponding to SATA Port 0. When used as an interlock switch status indication, this signal should be drive to '0' to indicate that the switch is closed and to '1' to indicate that the switch is open. If interlock switches are not required, this pin can be configured as GPIO21.
SATA1GP/ GPIO19	I	Serial ATA 1 General Purpose: Same function as SATA0GP, except for SATA Port 1. If interlock switches are not required, this pin can be configured as GPIO19.
SATA2GP/ GPIO36	I	Serial ATA 2 General Purpose: Same function as SATA0GP, except for SATA Port 2. If interlock switches are not required, this pin can be configured as GPIO36.

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Serial ATA Interface Signals (Continued)

Name	Type	Description
SATA3GP/ GPIO37	I	Serial ATA 3 General Purpose: Same function as SATA0GP, except for SATA Port 3. If interlock switches are not required, this pin can be configured as GPIO37.
SATALED#	OC	Serial ATA LED: This is an open-collector output pin driven during SATA command activity. It is to be connected to external circuitry that can provide the current to drive a platform LED. When active, the LED is on. When tri-stated, the LED is off. An external pull-up resistor to Vcc3_3 is required. NOTE: An internal pull-up is enabled only during PLTRST# assertion.
SATACLKREQ #/GPIO35	OD (Native)/ I/O (GP)	Serial ATA Clock Request: This is an open-drain output pin when configured as SATACLKREQ#. It is to connect to the system clock chip. When active, request for SATA Clock running is asserted. When tri-stated, it tells the Clock Chip that SATA Clock can be stopped. An external pull-up resistor is required.

Serial Peripheral Interface (SPI) Signals

Name	Type	Description
SPI_CS#	I/O	SPI Chip Select: Also used as the SPI bus request signal.
SPI_MISO	I	SPI Master IN Slave OUT: Data input pin for Intel® ICH7.
SPI_MOSI	O	SPI Master OUT Slave IN: Data output pin for ICH7.
SPI_ARB	I	SPI Arbitration: SPI arbitration signal is used to arbitrate the SPI bus with Intel PRO 82573E Gigabit Ethernet Controller when Shared Flash is implemented.
SPI_CLK	O	SPI Clock: SPI clock signal, during idle the bus owner will drive the clock signal low. 17.86 MHz.

Platform LAN Connect Interface Signals

Name	Type	Description
LAN_CLK	I	LAN I/F Clock: This signal is driven by the Platform LAN Connect component. The frequency range is 5 MHz to 50 MHz.
LAN_RXD[2:0]	I	Received Data: The Platform LAN Connect component uses these signals to transfer data and control information to the integrated LAN controller. These signals have integrated weak pull-up resistors.
LAN_TXD[2:0]	O	Transmit Data: The integrated LAN controller uses these signals to transfer data and control information to the Platform LAN Connect component.
LAN_RSTSYNC	O	LAN Reset/Sync: The Platform LAN Connect component's Reset and Sync signals are multiplexed onto this pin.

Other Clock

Name	Type	Description
CLK14	I	Oscillator Clock: This clock is used for 8254 timers. It runs at 14.31818 MHz. This clock is permitted to stop during S3 (or lower) states.
CLK48	I	48 MHz Clock: This clock is used to run the USB controller. Runs at 48.000 MHz. This clock is permitted to stop during S3 (or lower) states.
SATA_CLKP SATA_CLKN	I	100 MHz Differential Clock: These signals are used to run the SATA controller at 100 MHz. This clock is permitted to stop during S3/S4/S5 states.
DMI_CLKP, DMI_CLKN	I	100 MHz Differential Clock: These signals are used to run the Direct Media Interface. Runs at 100 MHz.

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IDE Interface Signals

Name	Type	Description
DCS1#	O	IDE Device Chip Selects for 100 Range: For ATA command register block. This output signal is connected to the corresponding signal on the IDE connector.
DCS3#	O	IDE Device Chip Select for 300 Range: For ATA control register block. This output signal is connected to the corresponding signal on the IDE connector.
DA[2:0]	O	IDE Device Address: These output signals are connected to the corresponding signals on the IDE connector. They are used to indicate which byte in either the ATA command block or control block is being addressed.
DD[15:0]	I/O	IDE Device Data: These signals directly drive the corresponding signals on the IDE connector. There is a weak internal pull-down resistor on DD7.
DDREQ	I	IDE Device DMA Request: This input signal is directly driven from the DRQ signal on the IDE connector. It is asserted by the IDE device to request a data transfer, and used in conjunction with the PCI bus master IDE function and are not associated with any AT compatible DMA channel. There is a weak internal pulldown resistor on this signal.
DDACK#	O	IDE Device DMA Acknowledge: This signal directly drives the DAK# signal on the IDE connector. DDACK# is asserted by the Intel® ICH7 to indicate to IDE DMA slave devices that a given data transfer cycle (assertion of DIOR# or DIOW#) is a DMA data transfer cycle. This signal is used in conjunction with the PCI bus master IDE function and are not associated with any AT-compatible DMA channel.
DIOR#/ (DWSTB/ RDMARDY#)	O	DIOR# /Disk I/O Read (PIO and Non-Ultra DMA): This is the command to the IDE device that it may drive data onto the DD lines. Data is latched by the ICH7 on the deassertion edge of DIOR#. The IDE device is selected either by the ATA register file chip selects (DCS1# or DCS3#) and the DA lines, or the IDE DMA acknowledge (DDAK#). Disk Write Strobe (Ultra DMA Writes to Disk): This is the data write strobe for writes to disk. When writing to disk, ICH7 drives valid data on rising and falling edges of DWSTB. Disk DMA Ready (Ultra DMA Reads from Disk): This is the DMA ready for reads from disk. When reading from disk, ICH7 deasserts RDMARDY# to pause burst data transfers.

IDE Interface Signals (Continued)

Name	Type	Description
DIOW#/ (DSTOP)	O	Disk I/O Write (PIO and Non-Ultra DMA): This is the command to the IDE device that it may latch data from the DD lines. Data is latched by the IDE device on the deassertion edge of DIOW#. The IDE device is selected either by the ATA register file chip selects (DCS1# or DCS3#) and the DA lines, or the IDE DMA acknowledge (DDAK#). Disk Stop (Ultra DMA): ICH7 asserts this signal to terminate a burst.
IORDY/ (DRSTB/ WDMARDY#)	I	I/O Channel Ready (PIO): This signal will keep the strobe active (DIOR# on reads, DIOW# on writes) longer than the minimum width. It adds wait-states to PIO transfers. Disk Read Strobe (Ultra DMA Reads from Disk): When reading from disk, ICH7 latches data on rising and falling edges of this signal from the disk. Disk DMA Ready (Ultra DMA Writes to Disk): When writing to disk, this is deasserted by the disk to pause burst data transfers.

System Management Interface Signals

Name	Type	Description
INTRUDER#	I	Intruder Detect: This signal can be set to disable system if box detected open. This signal's status is readable, so it can be used like a GPIO if the Intruder Detection is not needed.
SMLINK[1:0]	I/OD	System Management Link: SMBus link to optional external system management ASIC or LAN controller. External pull-ups are required. Note that SMLINK0 corresponds to an SMBus Clock signal, and SMLINK1 corresponds to an SMBus Data signal.
LINKALERT#	I/OD	SMLink Alert: Output of the integrated LAN and input to either the integrated ASF or an external management controller in order for the LAN's SMLINK slave to be serviced.

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USB Interface Signals

Name	Type	Description
USBP0P, USBP0N, USBP1P, USBP1N	I/O	Universal Serial Bus Port [1:0] Differential: These differential pairs are used to transmit Data/Address/Command signals for ports 0 and 1. These ports can be routed to UHCI controller #1 or the EHCI controller. NOTE: No external resistors are required on these signals. The Intel® ICH7 integrates 15 k Ω pull-downs and provides an output driver impedance of 45 Ω which requires no external series resistor.
USBP2P, USBP2N, USBP3P, USBP3N	I/O	Universal Serial Bus Port [3:2] Differential: These differential pairs are used to transmit data/address/command signals for ports 2 and 3. These ports can be routed to UHCI controller #2 or the EHCI controller. NOTE: No external resistors are required on these signals. The ICH7 integrates 15 K Ω pull-downs and provides an output driver impedance of 45 Ω which requires no external series resistor.
USBP4P, USBP4N, USBP5P, USBP5N	I/O	Universal Serial Bus Port [5:4] Differential: These differential pairs are used to transmit Data/Address/Command signals for ports 4 and 5. These ports can be routed to UHCI controller #3 or the EHCI controller. NOTE: No external resistors are required on these signals. The ICH7 integrates 15 K Ω pull-downs and provides an output driver impedance of 45 Ω which requires no external series resistor.
USBP6P, USBP6N, USBP7P, USBP7N	I/O	Universal Serial Bus Port [7:6] Differential: These differential pairs are used to transmit Data/Address/Command signals for ports 6 and 7. These ports can be routed to UHCI controller #4 or the EHCI controller. NOTE: No external resistors are required on these signals. The ICH7 integrates 15 K Ω pull-downs and provides an output driver impedance of 45 Ω which requires no external series resistor.
OC[4:0]# OC5#/GPIO29 OC6#/GPIO30 OC7#/GPIO31	I	Overcurrent Indicators: These signals set corresponding bits in the USB controllers to indicate that an overcurrent condition has occurred. OC[7:4]# may optionally be used as GPIOs. NOTE: OC[7:0]# are not 5 V tolerant.
USBRBIAS	O	USB Resistor Bias: Analog connection point for an external resistor. Used to set transmit currents and internal load resistors.
USBRBIAS#	I	USB Resistor Bias Complement: Analog connection point for an external resistor. Used to set transmit currents and internal load resistors.

EEPROM Interface Signals

Name	Type	Description
EE_SHCLK	O	EEPROM Shift Clock: Serial shift clock output to the EEPROM.
EE_DIN	I	EEPROM Data In: Transfers data from the EEPROM to the Intel® ICH7. This signal has an integrated pull-up resistor.
EE_DOUT	O	EEPROM Data Out: Transfers data from the ICH7 to the EEPROM.
EE_CS	O	EEPROM Chip Select: Chip select signal to the EEPROM.

Interrupt Signals

Name	Type	Description
SERIRQ	I/O	Serial Interrupt Request: This pin implements the serial interrupt protocol.
PIRQ[ID:A]#	I/OD	PCI Interrupt Requests: In non-APIC mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in the Interrupt Steering section. Each PIRQx# line has a separate Route Control register. In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQA# is connected to IRQ16, PIRQB# to IRQ17, PIRQC# to IRQ18, and PIRQD# to IRQ19. This frees the legacy interrupts.
PIRQ[H:E]#/ GPIO[5:2]	I/OD	PCI Interrupt Requests: In non-APIC mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in the Interrupt Steering section. Each PIRQx# line has a separate Route Control register. In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQE# is connected to IRQ20, PIRQF# to IRQ21, PIRQG# to IRQ22, and PIRQH# to IRQ23. This frees the legacy interrupts. If not needed for interrupts, these signals can be used as GPIO.
IDEIRQ	I	IDE Interrupt Request: This interrupt input is connected to the IDE drive.

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Power Management Interface Signals

Name	Type	Description
PWRBTN#	I	Power Button: The Power Button will cause SMI# or SCI to indicate a system request to go to a sleep state. If the system is already in a sleep state, this signal will cause a wake event. If PWRBTN# is pressed for more than 4 seconds, this will cause an unconditional transition (power button override) to the S5 state. Override will occur even if the system is in the S1-S4 states. This signal has an internal pullup resistor and has an internal 16 ms de-bounce on the input.
RI#	I	Ring Indicate: This signal is an input from a modem. It can be enabled as a wake event, and this is preserved across power failures.
SYS_RESET#	I	System Reset: This pin forces an internal reset after being debounced. The ICH7 will reset immediately if the SMBus is idle; otherwise, it will wait up to 25 ms $\pm$ 2 ms for the SMBus to idle before forcing a reset on the system.
LAN_RST#	I	LAN Reset: When asserted, the internal LAN controller will be put into reset. This signal must be asserted for at least 10 ms after the resume well power (VccSus3_3 and VccSus1_5) is valid. When de-asserted, this signal is an indication that the resume well power is stable. NOTE: LAN_RST# should be tied to RSMEST#.
WAKE#	I	PCI Express* Wake Event: Sideband wake signal on PCI Express asserted by components requesting wakeup.
MCH_SYNC#	I	MCH SYNC: This input is internally ANDed with the PWROK input. Connected to the ICH_SYNC# output of (G)MCH.
THRM#	I	Thermal Alarm: Active low signal generated by external hardware to generate an SMI# or SCL.
THRMTRIP#	I	Thermal Trip: When low, this signal indicates that a thermal trip from the processor occurred, and the ICH7 will immediately transition to a S5 state. The ICH7 will not wait for the processor stop grant cycle since the processor has overheated.
SUS_STAT#/ LPCPD#	O	Suspend Status: This signal is asserted by the ICH7 to indicate that the system will be entering a low power state soon. This can be monitored by devices with memory that need to switch from normal refresh to suspend refresh mode. It can also be used by other peripherals as an indication that they should isolate their outputs that may be going to powered-off planes. This signal is called LPCPD# on the LPC I/F.

Power Management Interface Signals (Continued)

Name	Type	Description
SUSCLK	O	Suspend Clock: This clock is an output of the RTC generator circuit to use by other chips for refresh clock.
RSMRST#	I	Resume Well Reset: This signal is used for resetting the resume power plane logic.
VRMPWRGD	I	VRM Power Good: This should be connected to be the processor's VRM Power Good signifying the VRM is stable. This signal is internally ANDed with the PWROK input.
PLTRST#	O	Platform Reset: The Intel® ICH7 asserts PLTRST# to reset devices on the platform (e.g., SIO, FWH, LAN, (G)MCH, IDE, TPM, etc.). The ICH7 asserts PLTRST# during power-up and when S/W initiates a hard reset sequence through the Reset Control register (I/O Register CF9h). The ICH7 drives PLTRST# inactive a minimum of 1 ms after both PWROK and VRMPWRGD are driven high. The ICH7 drives PLTRST# active a minimum of 1 ms when initiated through the Reset Control register (I/O Register CF9h). NOTE: PLTRST# is in the VccSus3_3 well.
SLP_S3#	O	S3 Sleep Control: SLP_S3# is for power plane control. This signal shuts off power to all non-critical systems when in S3 (Suspend To RAM), S4 (Suspend to Disk), or S5 (Soft Off) states.
SLP_S4#	O	S4 Sleep Control: SLP_S4# is for power plane control. This signal shuts power to all non-critical systems when in the S4 (Suspend to Disk) or S5 (Soft Off) state. NOTE: This pin must be used to control the DRAM power to use the ICH7's DRAM power-cycling feature. Refer to Chapter 5.14.10.2 for details.
SLP_S5#	O	S5 Sleep Control: SLP_S5# is for power plane control. This signal is used to shut power off to all non-critical systems when in the S5 (Soft Off) states.
PWROK	I	Power OK: When asserted, PWROK is an indication to the ICH7 that core power has been stable for 99 ms and that PCICLK has been stable for 1 ms. An exception to this rule is if the system is in S3HOT, in which PWROK may or may not stay asserted even though PCICLK may be inactive. PWROK can be driven asynchronously. When PWROK is negated, the ICH7 asserts PLTRST#. NOTE: PWROK must deassert for a minimum of three RTC clock periods for the ICH7 to fully reset the power and properly generate the PLTRST# output.

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Processor Interface Signals

Name	Type	Description
A20M#	O	Mask A20: A20M# will go active based on either setting the appropriate bit in the Port 92h register, or based on the A20GATE input being active.
CPUSLP#	O	CPU Sleep: This signal puts the processor into a state that saves substantial power compared to Stop-Grant state. However, during that time, no snoops occur. The Intel® ICH7 can optionally assert the CPUSLP# signal when going to the S1 state.
FERR#	I	Numeric Coprocessor Error: This signal is tied to the coprocessor error signal on the processor. FERR# is only used if the ICH7 coprocessor error reporting function is enabled in the OIC.CEN register (Chipset Config Registers:Offset 31FFh: bit 1). If FERR# is asserted, the ICH7 generates an internal IRQ13 to its interrupt controller unit. It is also used to gate the IGNNE# signal to ensure that IGNNE# is not asserted to the processor unless FERR# is active. FERR# requires an external weak pull-up to ensure a high level when the coprocessor error function is disabled. NOTE: FERR# can be used in some states for notification by the processor of pending interrupt events. This functionality is independent of the OIC register bit setting.
IGNNE#	O	Ignore Numeric Error: This signal is connected to the ignore error pin on the processor. IGNNE# is only used if the ICH7 coprocessor error reporting function is enabled in the OIC.CEN register (Chipset Config Registers:Offset 31FFh: bit 1). If FERR# is active, indicating a coprocessor error, a write to the Coprocessor Error register (I/O register F0h) causes the IGNNE# to be asserted. IGNNE# remains asserted until FERR# is negated. If FERR# is not asserted when the Coprocessor Error register is written, the IGNNE# signal is not asserted.
INIT#	O	Initialization: INIT# is asserted by the ICH7 for 16 PCI clocks to reset the processor. ICH7 can be configured to support processor Built In Self Test (BIST).
INIT3_3V#	O	Initialization 3.3 V: This is the identical 3.3 V copy of INIT# intended for Firmware Hub.
INTR	O	Processor Interrupt: INTR is asserted by the ICH7 to signal the processor that an interrupt request is pending and needs to be serviced. It is an asynchronous output and normally driven low.

Processor Interface Signals (Continued)

Name	Type	Description
NMI	O	Non-Maskable Interrupt: NMI is used to force a non-Maskable interrupt to the processor. The ICH7 can generate an NMI when either SERR# is asserted or IOCHK# goes active via the SERIRQ# stream. The processor detects an NMI when it detects a rising edge on NMI. NMI is reset by setting the corresponding NMI source enable/disable bit in the NMI Status and Control register (I/O Register 61h).
SMI#	O	System Management Interrupt: SMI# is an active low output synchronous to PCICLK. It is asserted by the ICH7 in response to one of many enabled hardware or software events.
STPCLK#	O	Stop Clock Request: STPCLK# is an active low output synchronous to PCICLK. It is asserted by the ICH7 in response to one of many hardware or software events. When the processor samples STPCLK# asserted, it responds by stopping its internal clock.
RCIN#	I	Keyboard Controller Reset CPU: The keyboard controller can generate INIT# to the processor. This saves the external OR gate with the ICH7's other sources of INIT#. When the ICH7 detects the assertion of this signal, INIT# is generated for 16 PCI clocks. NOTE: The ICH7 will ignore RCIN# assertion during transitions to the S3, S4, and S5 states.
A20GATE	I	A20 Gate: A20GATE is from the keyboard controller. The signal acts as an alternative method to force the A20M# signal active. It saves the external OR gate needed with various other chipsets.
CPUPWRGD/ GPIO49	O	CPU Power Good: This signal should be connected to the processor's PWRGOOD input to indicate when the CPU power is valid. This is an output signal that represents a logical AND of the ICH7's PWROK and VRMPWRGD signals. This signal may optionally be configured as a GPIO.

Firmware Hub Interface Signals

Name	Type	Description
FWH[3:0]/ LAD[3:0]	I/O	Firmware Hub Signals: These signals are multiplexed with the LPC address signals.
FWH4/ LFRAME#	O	Firmware Hub Signals: This signal is multiplexed with the LPC LFRAME# signal.

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General Purpose I/O Signals

Name	Type	Tolerance	Power Well	Description
GPIO49	I/O	V_CPU_IO	V_CPU_IO	Multiplexed with CPUPWRGD
GPIO48	I/O	3.3 V	Core	Multiplexed with GNT4#
GPIO[47:40]	N/A	3.3 V	N/A	Not implemented.
GPIO[39:38]	I/O	3.3 V	Core	Unmultiplexed.
GPIO37	I/O	3.3 V	Core	Multiplexed with SATA3GP.
GPIO36	I/O	3.3 V	Core	Multiplexed with SATA2GP.
GPIO35	I/O	3.3 V	Core	Multiplexed with SATACLKREQ#.
GPIO34	I/O	3.3 V	Core	Unmultiplexed.
GPIO33	I/O	3.3 V	Core	Unmultiplexed.
GPIO32	I/O	3.3 V	Core	Unmultiplexed.
GPIO31	I/O	3.3 V	Resume	Multiplexed with OC7#
GPIO30	I/O	3.3 V	Resume	Multiplexed with OC6#
GPIO29	I/O	3.3 V	Resume	Multiplexed with OC5#
GPIO28	I/O	3.3 V	Resume	Unmultiplexed.
GPIO27	I/O	3.3 V	Resume	Unmultiplexed.
GPIO26	I/O	3.3 V	Resume	Unmultiplexed.
GPIO25	I/O	3.3 V	Resume	Unmultiplexed.
GPIO24	I/O	3.3 V	Resume	Unmultiplexed. Not cleared by CF9h reset event.
GPIO23	I/O	3.3 V	Core	Multiplexed with LDRQ1#
GPIO22	I/O	3.3 V	Core	Multiplexed with REQ4#
GPIO21	I/O	3.3 V	Core	Multiplexed with SATA0GP.
GPIO20	I/O	3.3 V	Core	Unmultiplexed.
GPIO19	I/O	3.3 V	Core	Multiplexed with SATA1GP.
GPIO18	I/O	3.3 V	Core	Unmultiplexed.
GPIO17	I/O	3.3 V	Core	Multiplexed with GNT5#.
GPIO16	I/O	3.3 V	Core	Unmultiplexed.
GPIO[15:12]	I/O	3.3 V	Resume	Unmultiplexed.
GPIO11	I/O	3.3 V	Resume	Multiplexed with SMBALERT#
GPIO[10:8]	I/O	3.3 V	Resume	Unmultiplexed.
GPIO[7:6]	I/O	3.3 V	Core	Unmultiplexed.
GPIO[5:2]	I/OD	5 V	Core	Multiplexed with PIRQ[H:E]#.

General Purpose I/O Signals (Continued)

Name	Type	Tolerance	Power Well	Description
GPIO1	I/O	5 V	Core	Multiplexed with REQ5#.
GPIO0	I/O	3.3 V	Core	Unmultiplexed.

NOTES:

1. GPI[15:0] can be configured to cause a SMI# or SCI. Note that a GPI can be routed to either an SMI# or an SCI, but not both.
2. Some GPIOs exist in the VccSus3_3 power plane. Care must be taken to make sure GPIO signals are not driven high into powered-down planes. Some ICH7 GPIOs may be connected to pins on devices that exist in the core well. If these GPIOs are outputs, there is a danger that a loss of core power (PWROK low) or a Power Button Override event will result in the Intel ICH7 driving a pin to a logic 1 to another device that is powered down..

PCI Express* Signals

Name	Type	Description
PETp[1:4], PETn[1:4]	O	PCI Express* Differential Transmit Pair 1:4
PERp[1:4], PERn[1:4]	I	PCI Express Differential Receive Pair 1:4
PETp[5:6], PETn[5:6] (Intel® ICH7R Only)	O	PCI Express* Differential Transmit Pair 5:6 Reserved: ICH7
PERp[1:4], PERn[5:6] (ICH7R Only)	I	PCI Express Differential Receive Pair 5:6 Reserved: ICH7

SM Bus Interface Signals

Name	Type	Description
SMBDATA	I/OD	SMBus Data: External pull-up resistor is required.
SMBCLK	I/OD	SMBus Clock: External pull-up resistor is required.
SMBALERT#/ GPIO11	I	SMBus Alert: This signal is used to wake the system or generate SMI#. If not used for SMBALERT#, it can be used as a GPIO.

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AC'97/Intel® High Definition Auto Link Signals

Name	Type	Description
ACZ_RST#	O	AC'97/Intel® High Definition Audio Reset: Master hardware reset to external codec(s).
ACZ_SYNC	O	AC '97/Intel High Definition Audio Sync: 48 kHz fixed rate sample sync to the codec(s). Also used to encode the stream number.
ACZ_BIT_CLK	I/O	AC '97 Bit Clock Input: 12.288 MHz serial data clock generated by the external codec(s). This signal has an integrated pull-down resistor (see Note below). Intel High Definition Audio Bit Clock Output: 24.000 MHz serial data clock generated by the Intel High Definition Audio controller (the Intel® ICH7). This signal has an integrated pull-down resistor so that ACZ_BIT_CLK doesn't float when an Intel High Definition Audio codec (or no codec) is connected but the signals are temporarily configured as AC '97.
ACZ_SDOUT	O	AC '97/Intel High Definition Audio Serial Data Out: Serial TDM data output to the codec(s). This serial output is double-pumped for a bit rate of 48 Mb/s for Intel High Definition Audio. NOTE: ACZ_SDOUT is sampled at the rising edge of PWROK as a functional strap. See Function Straps for more details. There is a weak integrated pull-down resistor on the ACZ_SDOUT pin.
ACZ_SDIN[2:0]	I	AC '97/Intel High Definition Audio Serial Data In [2:0]: Serial TDM data inputs from the three codecs. The serial input is single-pumped for a bit rate of 24 Mb/s for Intel® High Definition Audio. These signals have integrated pulldown resistors, which are always enabled.

LPC Interface Signals

Name	Type	Description
LAD[3:0]/FWH[3:0]	I/O	LPC Multiplexed Command, Address, Data: For LAD[3:0], internal pull-ups are provided.
LFRAME#/FWH4	O	LPC Frame: LFRAME# indicates the start of an LPC cycle, or an abort.
LDRQ[0]#/LDRQ[1]#/GPIO23	I	LPC Serial DMA/Master Request Inputs: LDRQ[1:0]# are used to request DMA or bus master access. These signals are typically connected to external Super I/O device. An internal pull-up resistor is provided on these signals. LDRQ1# may optionally be used as GPIO.

Power and Ground Signals

Name	Description
Vcc3_3	3.3 V supply for core well I/O buffers (22 pins). This power may be shut off in S3, S4, S5 or G3 states.
Vcc1_05	1.05 V supply for core well logic (20 pins). This power may be shut off in S3, S4, S5 or G3 states.
Vcc1_5_A	1.5 V supply for Logic and I/O (30 pins). This power may be shut off in S3, S4, S5 or G3 states.
Vcc1_5_B	1.5 V supply for Logic and I/O (53 pins). This power may be shut off in S3, S4, S5 or G3 states.
V5REF	Reference for 5 V tolerance on core well inputs (2 pins). This power may be shut off in S3, S4, S5 or G3 states.
VccSus3_3	3.3 V supply for resume well I/O buffers (24 pins). This power is not expected to be shut off unless the system is unplugged in desktop configurations.
VccSus1_05	1.05 V supply for resume well logic (5 pins). This power is not expected to be shut off unless the system is unplugged in desktop configurations. This voltage may be generated internally (see Function Straps for strapping option). If generated internally, these pins should not be connected to an external supply.
V5REF_Sus	Reference for 5 V tolerance on resume well inputs (1 pin). This power is not expected to be shut off unless the system is unplugged in desktop configurations.
VccRTC	3.3 V (can drop to 2.0 V min. in G3 state) supply for the RTC well (1 pin). This power is not expected to be shut off unless the RTC battery is removed or completely drained. Note: Implementations should not attempt to clear CMOS by using a jumper to pull VccRTC low. Clearing CMOS in an Intel® ICH7-based platform can be done by using a jumper on RTCRST# or GPI.
VccUSBPLL	1.5 V supply for core well logic (1 pin). This signal is used for the USB PLL. This power may be shut off in S3, S4, S5 or G3 states. Must be powered even if USB not used.
VccDMIPLL	1.5 V supply for core well logic (1 pins). This signal is used for the DMI PLL. This power may be shut off in S3, S4, S5 or G3 states.
VccSATAPLL	1.5 V supply for core well logic (1 pins). This signal is used for the SATA PLL. This power may be shut off in S3, S4, S5 or G3 states. Must be powered even if SATA not used.
V_CPU_IO	Powered by the same supply as the processor I/O voltage (3 pins). This supply is used to drive the processor interface signals listed in Process Interface Signals .
Vss	Grounds (194 pins).

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5.3 Intel ICH7-M South Bridge (10)

Functional Strap Definitions

Signal	Usage	When Sampled	Description
GNT3#	Top-Block Swap Override	Rising Edge of PWROK	The signal has a weak internal pull-up. If the signal is sampled low, this indicates that the system is strapped to the “top-block swap” mode (Intel® ICH7 inverts A16 for all cycles targeting FWH BIOS space). The status of this strap is readable via the Top Swap bit (Chipset Config Registers:Offset 3414h:bit 0). Note that software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT2#	Reserved		This signal has a weak internal pull-up. NOTE: This signal should not be pulled low.
REQ[4:1]#	XOR Chain Selection	Rising Edge of PWROK	See Chapter 25 for functionality information.
LINKALERT#	Reserved		This signal requires an external pull-up resistor.
SPKR	No Reboot	Rising Edge of PWROK	The signal has a weak internal pull-down. If the signal is sampled high, this indicates that the system is strapped to the “No Reboot” mode (ICH7 will disable the TCO Timer system reboot feature). The status of this strap is readable via the NO REBOOT bit (Chipset Config Registers:Offset 3410h:bit 5).
INTVRMEN	Integrated VccSus1_05 VRM Enable/Disable	Always	Enables integrated VccSus1_05 VRM when sampled high.
EE_CS	Reserved		This signal has a weak internal pull-down. NOTE: This signal should not be pulled high.
EE_DOUT	Reserved		This signal has a weak internal pull-up. NOTE: This signal should not be pulled low.
GNT5#/ GPIO17#, GNT4#/ GPIO48	Boot BIOS Destination Selection	Rising Edge of PWROK	This field determines the destination of accesses to the BIOS memory range. Signals have weak internal pull-ups.Also controllable via Boot BIOS Destination bit (Chipset Config Registers:Offset 3410h:bit 11:10) (GNT5# is MSB) 01-SPI 10-PCI 11-LPC

Functional Strap Definitions (Continued)

Signal	Usage	When Sampled	Description
ACZ_SDOUT	XOR Chain Entrance/PCI Express* Port Config bit 1	Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK. See Chapter 25 for XOR Chain functionality information. When TP3 not pulled low at rising edge of PWROK, sets bit 1 of RPC.PC (Chipset Config Registers:Offset 224h). See Section 7.1.34 for details. This signal has a weak internal pull-down.
ACZ_SYNC	PCI Express Port Config bit 0	Rising Edge of PWROK	This signal has a weak internal pull-down. Sets bit 0 of RPC.PC (Chipset Config Registers:Offset 224h). See Section 7.1.34 for details.
GPIO25	Reserved	Rising Edge of RSMRST#	This signal has a weak internal pull-up. NOTE: This signal should not be pulled low.
GPIO16	Reserved		This signal has a weak internal pull-down. NOTE: This signal should not be pulled high.
SATALED#	Reserved		This signal has a weak internal pull-up enabled only when PLTRST# is asserted. NOTE: This signal should not be pulled low.
TP3	XOR Chain Entrance	Rising Edge of PWROK	See Chapter 25 for functionality information. This signal has a weak internal pull-up. NOTE: This signal should not be pulled low unless using XOR Chain testing.

Direct Media Interface Signals

Name	Type	Description
DMI[0:3]TXP, DMI[0:3]TXN	O	Direct Media Interface Differential Transmit Pair 0:3
DMI[0:3]RXP, DMI[0:3]RXN	I	Direct Media Interface Differential Receive Pair 0:3
DMI_ZCOMP	O	Impedance Compensation Input: Determines DMI input impedance.
DMI_IRCOMP	I	Impedance/Compensation Compensation Output: Determines DMI output impedance and bias current.

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5.3 Intel ICH7-M South Bridge (11)

Miscellaneous Signals

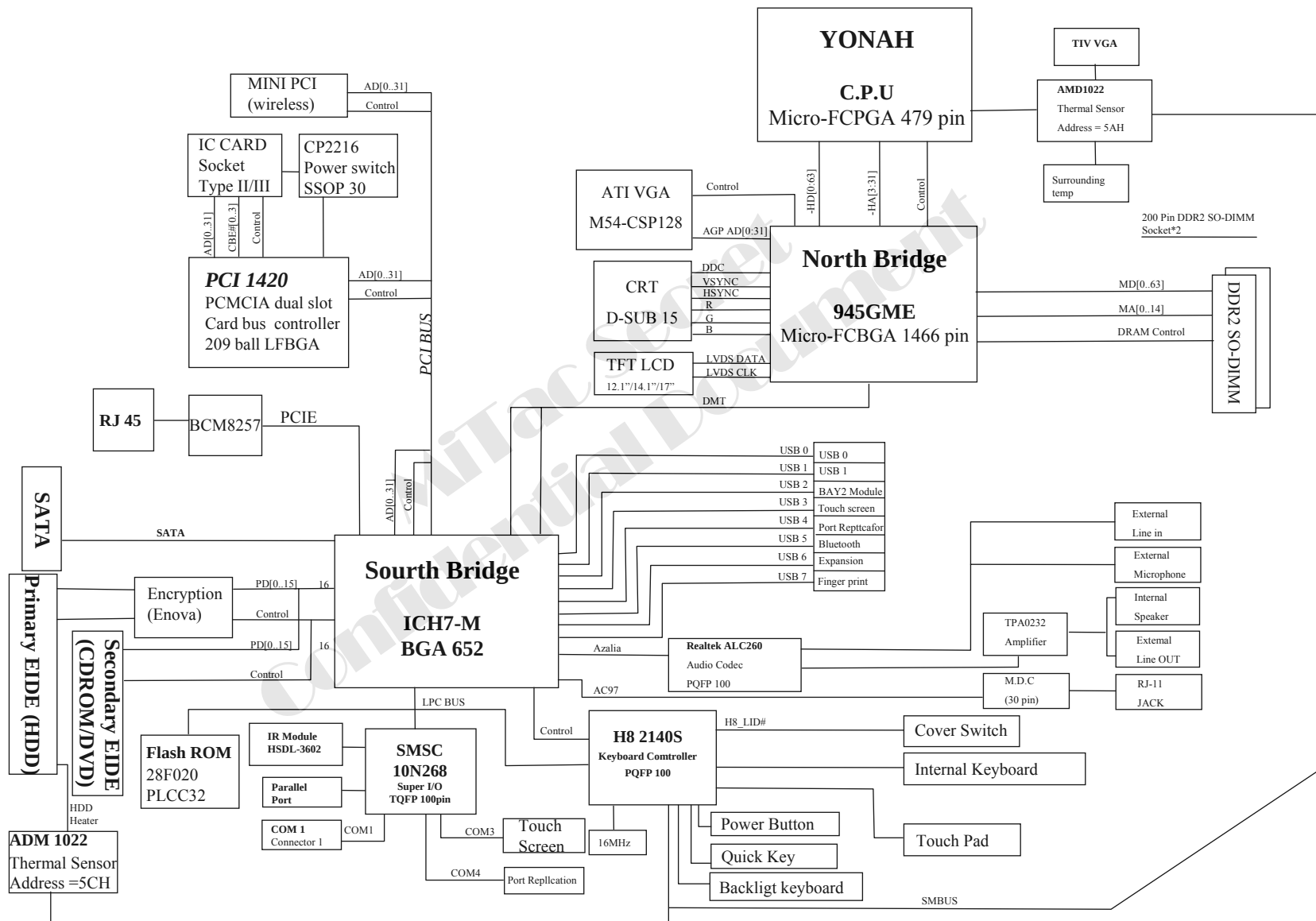
Name	Type	Description
INTVRMEN	I	Internal Voltage Regulator Enable: This signal enables the internal 1.05 V Suspend regulator when connected to VccRTC. When connected to Vss, the internal regulator is disabled.
SPKR	O	Speaker: The SPKR signal is the output of counter 2 and is internally “ANDed” with Port 61h bit 1 to provide Speaker Data Enable. This signal drives an external speaker driver device, which in turn drives the system speaker. Upon PLTRST#, its output state is 0. NOTE: SPKR is sampled at the rising edge of PWROK as a functional strap. See Function Straps for more details. There is a weak integrated pull-down resistor on SPKR pin.
RTCRST#	I	RTC Reset: When asserted, this signal resets register bits in the RTC well. NOTES: 1. Unless CMOS is being cleared (only to be done in the G3 power state), the RTCRST# input must always be high when all other RTC power planes are on. 2. In the case where the RTC battery is dead or missing on the platform, the RTCRST# pin must rise before the RSMRST# pin.
TP0	I	Test Point 0: This signal must have an external pull-up to VccSus3 3.
TP1	O	Test Point 1: Route signal to a test point.
TP2	O	Test Point 2: Route signal to a test point.
TP3	I/O	Test Point 3: Route signal to a test point.

Real Time Clock Interface

Name	Type	Description
RTCX1	Special	Crystal Input 1: This signal is connected to the 32.768 KHz crystal. If no external crystal is used, then RTCX1 can be driven with the desired clock rate.
RTCX2	Special	Crystal Input 2: This signal is connected to the 32.768 KHz crystal. If no external crystal is used, then RTCX2 should be left floating.

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6. System Block Diagram



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7. Maintenance Diagnostics

7.1 Introduction

Each time the computer is turned on, the system BIOS runs a series of internal checks on the hardware. This power-on self test (post) allows the computer to detect problems as early as the power-on stage. Error messages of post can alert you to the problems of your computer.

If an error is detected during these tests, you will see an error message displayed on the screen. If the error occurs before the display is initialized, then the screen cannot display the error message. Error codes or system beeps are used to identify a post error that occurs when the screen is not available.

The value for the diagnostic port is written at the beginning of the test. Therefore, if the test failed, the user can determine where the problem occurred by reading the last value written to the port by the Mini PCI-E card plug at Mini PCI-E slot.

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7.2 Error Codes (1)

Following is a list of error codes in sequent display on the Mini PCI-E debug board.

Tpoint	Hook Routine	Post Routine	Description
02h	hookVerifyRealModeJ	postVerifyRealModeJ (Stackless-No Memory)	Verify Real Mode. If the CPU is in protected mode, turn on A20 and pulse the reset line, forcing a shutdown 0.NOTE: Hook routine should not alter DX, which holds the powerup CPU ID.
03h	hookDisableNmiJ	postDisableNmiJ	Disable Non-Maskable Interrupts.
04h	hookCpuGetTypeJ	CpuGetTypeJ (Stackless)	Get CPU type from CPU registers and other methods. Save CPU type in NVRAM.NOTE: Hook routine should not alter DX, which holds the powerup CPU ID.
06h	hookHardwareInitJ	postHardwareInitializeJ (Stackless)	Initialize system hardware. Reset the DMA controllers, disable the videos, clear any pending interrupts from the real-time clock and set up port B register.
07h	hookCsBiosDeshadowJ	csBiosDeshadowJ (Stackless, Optional)	Disable system ROM shadow and start to execute ROMEXEC code from the flash part. This task is pulled into the build only when the ROMEXEC relocation is installed.
08h	hookChipsetInitJ	csInitializeJ (Stackless)	Initialize chip set registers to the Initial
09h	hookSetInPostFlagJ	postSetInPostFlagJ	Set in-POST flag in CMOS that indicates we are in POST. If this bit is not cleared by postClearBootFlagJ (AEh), the TrustedCore on next boot determines that the current configuration caused POST to fail and uses default values for configuration. Clear the
0Ah	hookCpuInitialize1J (Warm) hookCpuInitialize2J (Cold)	cpuInitializeJ (Stackless)	Initialize CPU registers

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7.3 Error Codes (2)

Following is a list of error codes in sequent display on the Mini PCI-E debug board.

Tpoint	Hook Routine	Post Routine	Description
0Bh	hookCpuCacheOnJ	cpuCacheOnJ	Enable CPU cache. Set bits in cmos related to cache.
0Ch	hookCacheInitializeJ	cacheInitializeJ (Stackless)	Set the initial POST values of the cache registers if not integrated into the chipset.
0Eh	hookIoInitializeJ	ioInitializeJ (Stackless, optional)	Set the initial POST values for registers in the integrated I/O chip.
0Fh	hookfDiskInitializeJ	fdiskInitializeJ	Enable the local bus IDE as primary or secondary depending on other drives
10h	hookPmInitializeJ	pmInitializeJ (Optional)	Initialize Power Management.
11h	hookRegInitJ	postRegInitializeJ (Stackless, optional)	General dispatcher for alternate register initialization. Set initial POST values for other hardware devices defined in the register tables.
12h	hookRestoreCR0J	cpuRestoreCR0J (Stackless-No memory)	Restore the contents of the CPU control word whenever the CPU is reset.
13h	hookPciBusMasterResetJ	pciBusMasterResetJ (Warm start, optional)	Early reset of PCI devices required to disable bus master. Assumes the presence of a stack and running from decompressed shadow memory.
14h	hookI8742InitJ	postI8742InitJ (Stackless)	Verify that the 8742 keyboard controller is responding. Send a self-test command to the 8742 and wait for results. Also read the switch inputs from the 8742 and write the keyboard controller command byte.
16h	hookChecksumTestJ	postChecksumTestJ (Stackless)	Verify that the ROM BIOS checksums to zero
17h	hookCachePreRamAutoSizeJ	cachePreRamAutoSizeJ (Stackless, Optional)	Initialize external cache before autosizing memory.

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7.3 Error Codes (3)

Following is a list of error codes in sequent display on the Mini PCI-E debug board.

Tpoint	Hook Routine	Post Routine	Description
18h	hookTimerInitJ	postTimerInitJ (Stackless)	Initialize all three of the 8254 timers. Set the clock timer (0) to binary count, mode 3 (square wave mode), and read/write LSB then MSB. Initialize the clock timer to zero. Set the RAM refresh timer (1) to binary count, mode 2 (Rate Generator), and read/
1Ah	hookDmaInitJ	postDmaInitJ	Initialize DMA command register with these settings: 1. Memory to memory disabled 2. Channel 0 hold address disabled 3. Controller enabled 4. Normal timing 5. Fixed priority 6. Late write selection 7. DREQ sense active 8. DACK sense active low. Initialize
1Ch	hookResetICsJ	postResetICsJ (Stackless)	Initialize interrupt controllers for some shutdowns.
20h	hookRefreshTestJ	postRefreshTestJ (Stackless)	Verify that DRAM refresh is operating by polling the refresh bit in PORTB.
22h	hookWarmKBStartJJ	postWarmKBStartJ (Stackless)	Reset the keyboard.
24h	hookSetHugeESJ (Stackless)hookSetHugeES2J	postSetHugeESJ	Set segment-register addressability to 4 GB
28h	hookRamAutosizeJ	csRamAutosizeJ (Stackless)	Using the table of configurations supplied by the specific chipset module, test each DRAM configuration to see if that particular configuration is valid. Then program the chipset to its autosized configuration. Before autosizing, disable all caches and al
29h	hookPostMemoryMgrInitJ	postMemoryMgrInitJ	Initialize the POST Memory Manager

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7.3 Error Codes (4)

Following is a list of error codes in sequent display on the Mini PCI-E debug board.

Tpoint	Hook Routine	Post Routine	Description
2Ah	hookZeroBaseRamJ	postZeroBaseRamJ (Stackless)	Zero the first 512 K of RAM
2Ch	hookRealAddressTestJ	postRealAddressTestJ (Stackless)	Test 512 K base address lines
2Eh	hookBaseRamTestJ	postBaseRamTestJ (Stackless)	Test first 512 K of RAM.
2Fh	hookCachePreSysShadowJ	cachePreSysShadowJ (Stackless)	Initialize external cache before shadowing.
32h	hookComputeSpeedJ	cpuComputeSpeedJ	Compute CPU speed.
33h	hookPdmInitJ	postPdmInitJ	Initialize the Phoenix Dispatch Manager
36h	hookCheckShutdownCodeJ	postCheckShutdownCodeJ (Stackless-No Memory)	Vector to proper shutdown routine.
38h`	hookSysShadowConfigJ	csSysShadowConfigJ	Shadow the system BIOS.
3Ah	hookCacheAutosizeJ	CacheAutosizeJ	Autosize external cache and program cache size for enabling later in POST.
3Ch	hookAdvCsConfigJ	csAdvConfigJ (Optional)	If CMOS is valid, load chipset registers with values from CMOS, otherwise load defaults and display Setup prompt. If Auto Configuration is enabled, always load the chipset registers with the Setup defaults (Rel 6.0).
3Dh	hookAdvRegConfigJ	postAdvRegConfigJ (Optional)	Load alternate registers with CMOS values.
41h	hookRomPilotInitJ	featRomPilotInitJ	Initialize extended memory for RomPilot.
42h	hookVectorInitJ	postVectorInitJ (Stackless)	Initialize interrupt vectors 0 thru 77h to the TrustedCore general interrupt handler.
45h	hookCoreDeviceInitJ	coreDeviceInitJ	Initialize all motherboard devices.
46h	hookCopyrightCheckJ	postCopyrightCheckJ	Verify the ROM copyright notice

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7.3 Error Codes (5)

Following is a list of error codes in sequent display on the Mini PCI-E debug board.

Tpoint	Hook Routine	Post Routine	Description
47h	hookI2oInitJ	i2oInitJ (Optional)	Initialize support for I2O by initializing global variables used by the I2O code. Pause POST table processing if a CMOS bit is set (for debugging).
48h	hookConfigCheckJ	postConfigCheckJ	Verify that the equipment specified in the CMOS matches the hardware currently installed. If the monitor type is set to 00 then a video ROM must exist. If the monitor type is 1 or 2 set the video switch to CGA. If monitor type 3, set the video switch to m
49h	hookPciInitJ	pciInitJ	Perform these tasks:1. Size the PCI bus topology and set bridge bus numbers.2. Set the system max bus number.3. Write a 0 to the command register of every PCI device.4. Write a 0 to all 6 base registers in every PCI device.5. Write a -1 to the status regi
4Ah	hookVideoInitJ	pciVideoInitJ	Initialize all video adapters in system
4Bh	hookQuietBootStartJ	quietBootStartJ (Optional)	Initialize QuietBoot if it is installed. Enable both keyboard and timer interrupts (IRQ0 and IRQ1). If your POST tasks require interrupts off, preserve them with a PUSHF and CLI at the beginning and a POPF at the end. If you change the PIC, preserve the e
4Ch	hookVidShadowConfigJ	csVidShadowConfigJ	Shadow video BIOS ROM if specified by Setup, and CMOS is valid and the previous boot was OK.
4Eh	hookCopyrightDisplayJ	postCopyrightDisplayJ	Display copyright notice.

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7.3 Error Codes (6)

Following is a list of error codes in sequent display on the Mini PCI-E debug board.

Tpoint	Hook Routine	Post Routine	Description
4Fh	hookMultiBootInitJ	multiBootInitFarJ (Optional)	Initialize MultiBoot. Allocate memory for old and new MultiBoot history tables.
50h	hookCpuDisplayJ	CpuDisplayJ	Display CPU type and speed
51h	hookEisaInitJ	eisaInitJ	Checksum CMOS and initialize each EISA slot with data from the initialization data block.
52h	hookWarmKBTestJ	postWarmKBTestJ	Verify keyboard reset.
52h	hookKBTestJ	postKBTestJ	Verify keyboard reset.
54h	hookSetupKeyclickJ	featSetupKeyclickJ (Optional)	Initialize keystroke clicker if enabled in Setup.
55h	hookUsbConfigUsbFarJ	usbConfigUsbFarJ (Optional)	Enable USB devices.
58h	hookHotInterruptTestJ	postHotInterruptTestJ	Test for unexpected interrupts. First do an STI for hot interrupts. Secondly, test the NMI for an unexpected interrupt. Thirdly, enable the parity checkers and read from memory, checking for an unexpected interrupt.
59h	hookPdsInitializeJ	pdsInitializeJ (Optional)	Register POST Display Services, fonts, and languages with the POST Dispatch Manager.
5Ah	hookDisplayF2MessageJ	postDisplayF2MessageJ	Display prompt "Press F2 to enter SETUP"
5Bh	hookCpuCacheOffJ	cpuCacheOffJ (Stackless)	Disable CPU cache.
5Ch	hookMemoryTestJ	postMemoryTestJ	Test RAM between 512K and 640K.

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7.3 Error Codes (7)

Following is a list of error codes in sequent display on the Mini PCI-E debug board.

Tpoint	Hook Routine	Post Routine	Description
60h	hookExtendedMemoryTestJ	postExtendedMemoryTestJ	Determine and test the amount of extended memory available. Determine if memory exists by writing to a few strategic locations and see if the data can be read back. If so, perform an address-line test and a RAM test on the memory. Save the total extended
62h	hookExtendedAddressTestJ	postExtendedAddressTestJ	Perform an address line test on A0 to the amount of memory available. This test is dependent on the processor, since the test will vary depending on the width of memory (16 or 32 bits). This test will also use A20 as the skew address to prevent corruption
64h	hookUserPatch1J	postUserPatch1J	Jump to UserPatch1. See "The POST Component."
66h	hookAdvCacheConfigJ	cacheAdvConfigJ (Optional)	Set cache registers to their CMOS values if CMOS is valid, unless auto configuration is enabled, in which case load cache registers from the Setup default table.
67h	hookMpInitMinJ	mpInitMinJ (Optional)	Quick initialization of all Application Processors in a multi-processor system.
68h	hookCacheConfigureJ	cacheConfigureJ	Enable external cache and CPU cache if present. Configure non-cacheable regions if necessary. NOTE: Hook routine must preserve DX, which carries the cache size to the DisplayCacheSizeJ routine.
69h	hookPmSMMInitJJ	pmSMMInitJ (Optional)	Initialize the handler for SMM.

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7.3 Error Codes (8)

Following is a list of error codes in sequent display on the Mini PCI-E debug board.

Tpoint	Hook Routine	Post Routine	Description
6Ah	hookDisplayCacheSizeJ	postDisplayCacheSizeJ	Display external cache size on the screen if it is non-zero.NOTE: Hook routine must preserve DX, which carries the cache size from the cacheConfigureJ routine.
6Bh	hookLoadCustomDefaultsJ	featLoadCustomDefaultsJ (Optional)	If CMOS is bad, load Custom Defaults from flash into CMOS. If successful, reboot.
6Ch	hookDisplayShadowsJ	postDisplayShadowsJ	Display shadow message
6Eh	hookDisplayNonDispJ	postDisplayNonDisposab leJ	Display the starting offset of the non-disposable segment of TrustedCore
70h	hookDisplayErrorMsgsJ	postDisplayErrorMessage sJ	Check flags in CMOS and in the TrustedCore data area for errors detected during POST. Display error messages on the screen.
72h	hookTestConfigJ	postTestConfigJ	Check status bits to see if configuration problems were detected. If so, display error messages on the screen.
76h	hookKeyboardTestJ	postKeyboardTestJ	Check status bits for keyboard-related failures. Display error messages on the screen.
7Ch	hookSetupHW VectorsJ	postSetupHardwareVecto rsJ	Initialize the hardware interrupt vectors from 08 to 0F and from 70h to 77H. Also set the interrupt vectors from 60h to 66H to zero.
7Dh	hookISMInitJ	postISMInitJ (Optional)	Initialize Intelligent System Monitoring.
7Eh	hookCoproprocessorTestJ	cpuCoproprocessorTestJ	The Coprocessor initialization test. Use the floating point instructions to determine if a coprocessor exists instead of the ET bit in CR0.

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7.3 Error Codes (9)

Following is a list of error codes in sequent display on the Mini PCI-E debug board.

Tpoint	Hook Routine	Post Routine	Description
80h	hookIoBeforeInitJ	ioBeforeInitJ (Optional)	Disable onboard COM and LPT ports before testing for presence of external I/O devices..
81h	hookCoreLateDeviceInitJ	corelateDeviceInitJ (Optional)	Run late device initialization routines.
82h	hookRS232TestCodeJ	ioRS232TestCodeJ	Test and identify RS232 ports.
83h	hookFdiskCfgIdeCtrlrJ	fdiskCfgIdeCtrlrJ	Configure Fisk Disk Controller.
84h	hookParallelTestCodeJ	ioParallelTestCodeJ	Test and identify parallel ports.
85h	hookPciInitPccJ	pciInitPccJ (Optional)	Display any ESCD read errors and configure all PnP ISA devices.
86h	hookIoAfterInitJ	ioAfterInitJ (Optional)	Initialize onboard I/O and BDA according to CMOS and presence of external devices.
87h	hookMcdConfigureDevicesJ	mcdPostConfigureDevicesJ	Initialize motherboard configurable devices.
88h	hookBiosInitJ	postBiosInitJ	Initialize interrupt controller.
89h	hookEnableNmiJ	postEnableNmiJ	Enable non-maskable interrupts.
8Ah	hookInitExtBDAJ	postInitExtBDAJ	Initialize Extended BIOS Data Area and initialize the mouse.
8Bh	hookMouseTestJ	featMouseTestJ (Optional)	Setup interrupt vector and present bit in Equipment byte.
8Ch	hookFloppyTestJ	postFloppyTestJ	Initialize both of the floppy disks and display an error message if failure was detected. Check both drives to establish the appropriate diskette types in the TrustedCore data area.
8Fh	hookFdiskPreFastInitJ,	fdiskPreFastInitJ (Optional)	Count the number of ATA drives in the system and update the number in bdaFdiskcount.

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7.3 Error Codes (10)

Following is a list of error codes in sequent display on the Mini PCI-E debug board.

Tpoint	Hook Routine	Post Routine	Description
90h	hookFDiskTestJ	fdiskPostTestJ	Initialize hard-disk controller. If the CMOS ram is valid and intact, and fixed disks are defined, call the fixed disk init routine to initialize the fixed disk system and take over the appropriate interrupt vectors.
91h	hookFdiskFastInitJ	fdiskFastInitJ (Optional)	Configure the local bus IDE timing register based on the drives attached to it.
92h	hookUserPatch2J	userPatch2J	Jump to UserPatch2. See "The POST Component".
93h	hookMpInitJ	mpInitJ (Optional)	Build the MPTABLE for multi-processor
95h	hookCDTestJ	hddCDTestJ (Optional)	1. Check CMOS for CD-ROM drive present 2. Activate the drive by checking for media present 3. Check sector 11h (17) for Boot Record Volume Descriptor 4. Check the boot catalog for validity 5. Pick a boot entry 6. Create a Specification Packet
96h	hookClearHugeESJ	postDoShutdown8	Reset segment-register addressability from 4GB to normal 64K by generating a Shutdown 8.
97h	hookMpFixUpTableJ	postMpFixUpTableJ (Optional)	Create pointer to MP table in Extended BDA.
98h	hookRomAreaCheckJ	postRomAreaCheckJ	Search for option ROMs. Rom scan the area from C800h for a length of BCP_ROM_Scan_Size (or to E000h by default) on every 2K boundary, looking for add on cards that need initialization.
99h	hookCheckSmartJ	postCheckSmartJ (Optional)	Check support status for Self-Monitoring Analysis Reporting Technology (disk-failure warning).

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7.3 Error Codes (11)

Following is a list of error codes in sequent display on the Mini PCI-E debug board.

Tpoint	Hook Routine	Post Routine	Description
9Ah	hookMiscShadowConfigJ	csMiscShadowConfigJ	Shadow miscellaneous ROMs if specified by Setup and CMOS is valid and the previous boot was OK.
9Ch	hookPmSetupJ (Optional)	pmSetupJ	Set up Power Management. Initiate power - management state machine.
9Dh	hookSecurityEngineInitJ	securityEngineInitJ (Optional)	Initialize Security Engine.
9Eh	hookEnableIRQsJ	postEnableIRQsJ	Enable hardware interrupts
9Fh	hookFdiskRestFastInitJ	fdiskRestFastInitJ (Optional)	Check the total number of Fast Disks (ATA and SCSI) and update the bdaFdiskCount.
A0h	hookSetTimeOfDayJ	postSetTimeOfDayJ	Verify that the system clock is interrupting.
A2h	hookKeyLockTestJ	postKeyLockTestJ	Setup Numlock indicator. Display a message if key switch is locked.
A4h	hookInitKeyRateJ	featInitKeyboardRateJ (Optional)	Initialize typematic rate
A8h	hookEraseF2MsgJ	postEraseF2MsgJ	Overwrite the "Press F2 for Setup" prompt with spaces, erasing it from the screen.
AAh	hookScanForF2J	postScanForF2J	Scan the key buffer to see if the F2 key was struck after keyboard interrupts were enabled. If an F2 keystroke is found, set a flag.
ACh	hookSetupCheckJ	postSetupCheckJ	Enter SETUP. If (F2 was pressed) go to SETUP Else if (errors were found) display "Press F1 or F2" prompt if (F2 is pressed) go to setup else if (F1 is pressed) boot Else boot
A Eh	hookClearBootFlagJ	postClearBootFlagJ	Clear ConfigFailedBit and InPostBit in CMOS.

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7.3 Error Codes (12)

Following is a list of error codes in sequent display on the Mini PCI-E debug board.

Tpoint	Hook Routine	Post Routine	Description
B0h	hookErrorCheckJ	postErrorCheckJ	Check for errors. If (errors were found) beep twice display "F1 or F2" message if (F2 keystroke) go to SETUP if (F1 keystroke) go to BOOT
B1h	hookRomPilotUnloadJ	featRomPilotUnloadJ	Inform RomPilot about the end of POST.
B2h	hookPostDoneJ	postDoneJ	Change status bits in CMOS and/or the TrustedCore data area to reflect the fact that POST is complete.
B4h	hookOneBeepJ	postOneBeepJ	One quick beep
B5h	hookQuietBootEndJ	quietBootEndJ (Optional)	Turn off <Esc> and <F2> key checking. IF (VGA adapter is present) IF (OEM screen is still up) Note OEM screen is gone. Fade out OEM screen. Reset video: clear screen, reset cursor, reload DAC. ENDIF ENDIF
B6h	hookCheckPasswordJ	featCheckPasswordJ (Optional)	If password on boot is enabled, a call is made to Setup to check password. If the user does not enter a valid password, Setup does not return.
B7h	hookACPIConfigJJ	postACPIConfigJ	Initialize ACPI BIOS.
B9h	hookPrepareToBoot	postPrepareToBootj	Clear all screen graphics before booting.
BAh	hookDMICongigJ	postDMICongigJ (Optional)	Initialize the SMBIOS header and sub-structures.
BCh	hookClearParityJ	postClearParityJ	Clear parity-error latch
BDh	hookBootMenuJ	featBootMenuJ (Optional)	Display Boot First menu if MultiBoot is installed.
BEh	hookClearScreenJ	postClearScreenJ	If BCP option is enabled, clear the screen before booting.

A790 N/B Maintenance

7.3 Error Codes (13)

Following is a list of error codes in sequent display on the Mini PCI-E debug board.

Tpoint	Hook Routine	Post Routine	Description
BFh	hookCheckRemindersJ	postCheckRemindersJ	Check virus and backup reminders. Display
C0h	hookInt19	postInt19	Try to boot with INT 19
C1h	hookPemInit	pemInitFarJ	Initialize the Post Error Manager.
C2h	hookPemLog	pemLogErrorsFarJ	Write PEM errors.
C3h	hookPemDisplay	pemDisplayErrorsFarJ	Display PEM errors.
C4h	hookPemSuserInit	pemSysInitJ (Stackless)	Initialize system error handler
C5h	hookPnpndDualCmosJ	Initialize note dock	PnPnd dual CMOS optional
C6h	hookNotedockInitJ	postNotedockInitJ (Optional)	Initialize note dock
C7h	hookNotedockInitLate	postNotedockInitLateJ (Optional)	Initialize note dock late
C8h	hookForceCheckJ	postForceCheckJ	Force check (optional)
C9h	hookExtendedChecksumBI	postExtendedChecksumBI OSJ	Extended checksum (optional)
CAh	hookSerKeyInitJJ	featSerKeyInitJ (Optional)	Redirect Int 15h to enable target board to use remote keyboard (PICO BIOS).
CBh	hookRomRamTestJ	featRomRamTestJ (Optional)	Redirect Int 13h to Memory Technologies Devices such as ROM, RAM, PCMCIA, and serial disk (PICO BIOS).
CCh	hookSerVidInitJ	featSerVidInitJ (Optional)	Redirect Int 10h to enable target board to use a remote serial video (PICO BIOS).
CDh	hookPcmAtaTestJ	featPcmAtaTestJ (Optional)	Remap I/O and memory address space for PCMCIA (PICO BIOS).
CEh	hookPenInitJ	penInitJ (Optional)	Initialize digitizer device and display installed message if successful.

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8. Trouble Shooting

- ☐ **8.1 No Power (*1)**
- ☐ **8.2 No Display (*2)**
- ☐ **8.3 Graphics Controller Test Error LCD No Display**
- ☐ **8.4 External Monitor No Display**
- ☐ **8.5 Memory Test Error**
- ☐ **8.6 Keyboard (K/B) or Touch-Pad (T/P) Test Error**
- ☐ **8.7 Hard Drive Test Error**
- ☐ **8.8 USB Port Test Error**
- ☐ **8.9 Mini-PCI Socket Test Error**
- ☐ **8.10 Audio Test Error**
- ☐ **8.11 LAN Test Error**
- ☐ **8.12 Modem Test Error**
- ☐ **8.13 Finger Print Board Test Error**

A790 N/B Maintenance

***1: No Power Definition**

Base on ACPI Spec. We define the no power as while we press the power button, the system can't leave S5 status or none the PG signal send out from power supply.

Judge condition:

- Check whether there are any voltage feedback control to turn off the power
- Check whether no CPU power will cause system can't leave S5 status

If there are not any diagram match these condition, we should stop analyzing the schematic in power supply sending out the PG signal. If yes, we should add the effected analysis into no power chapter.

***2: No Display Definition**

Base on the digital IC three basic working conditions: working power, reset, Clock. We define the no display as while system leave S5 status but can't get into S0 status.

Judge condition:

- Check which power will cause no display
- Check which reset signal will cause no display
- Check which Clock signal will cause no display

Base on these three conditions to analyze the schematic and edit the no display chapter.

Keyword:

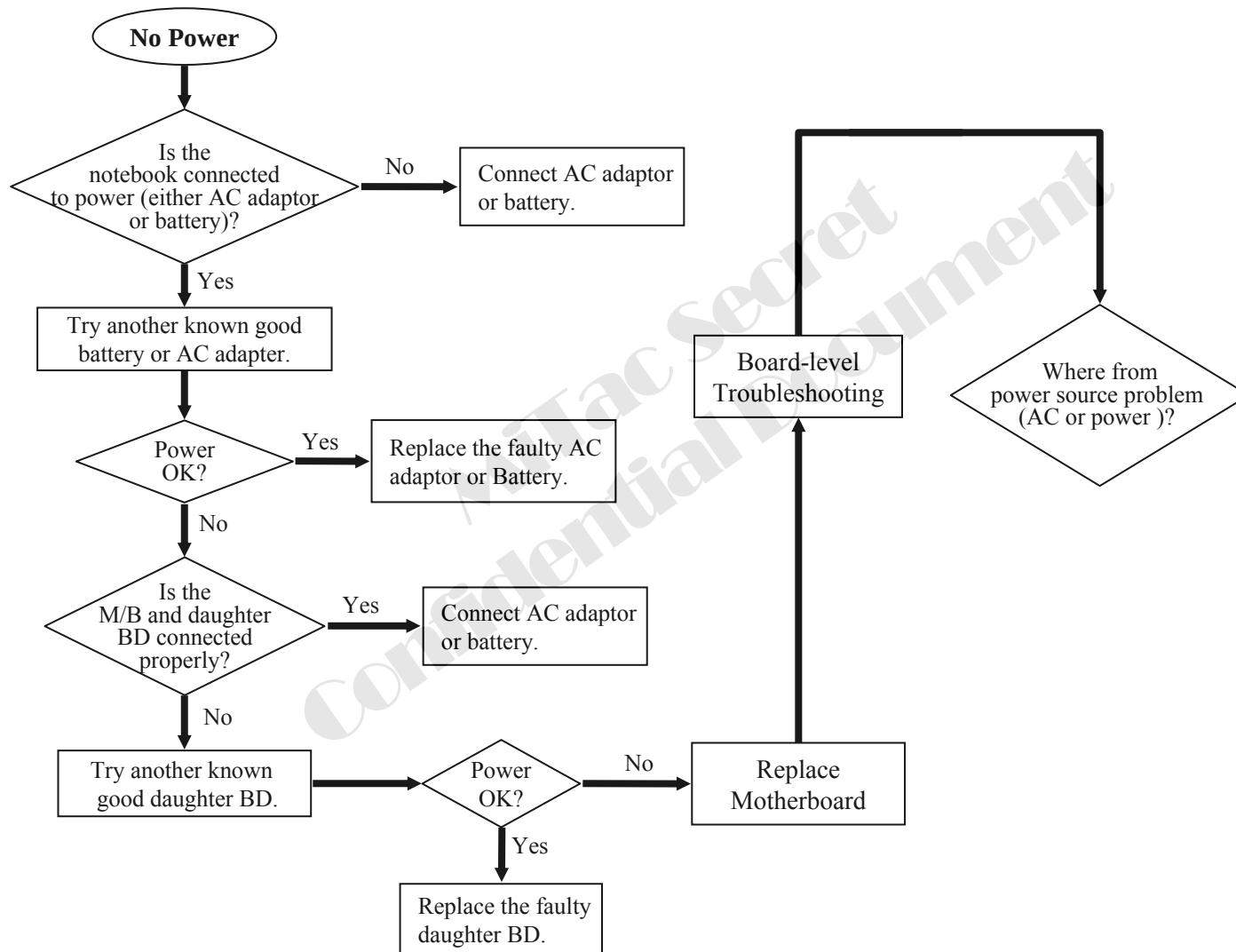
- S5: *Soft Off*
- S0: *Working*

For detail please refer the ACPI specification.

A790 N/B Maintenance

8.1 No Power-1

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.

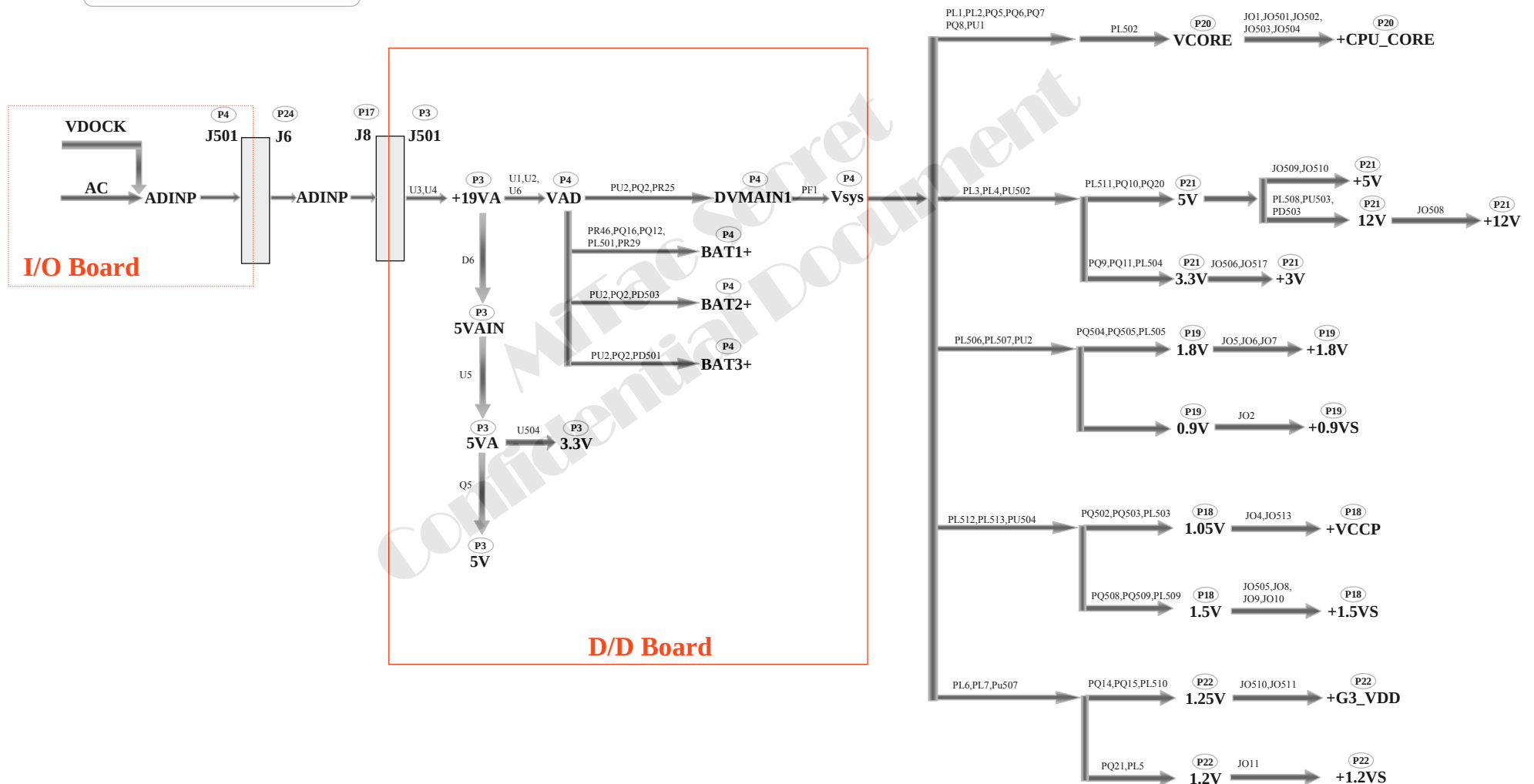


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8.1 No Power-2

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.

Main Voltage Map



8.1 No Power-3

The schematic diagram illustrates the internal structure and external components of the OZ806 power management IC. The IC is a 16-pin device with the following pins and connections:

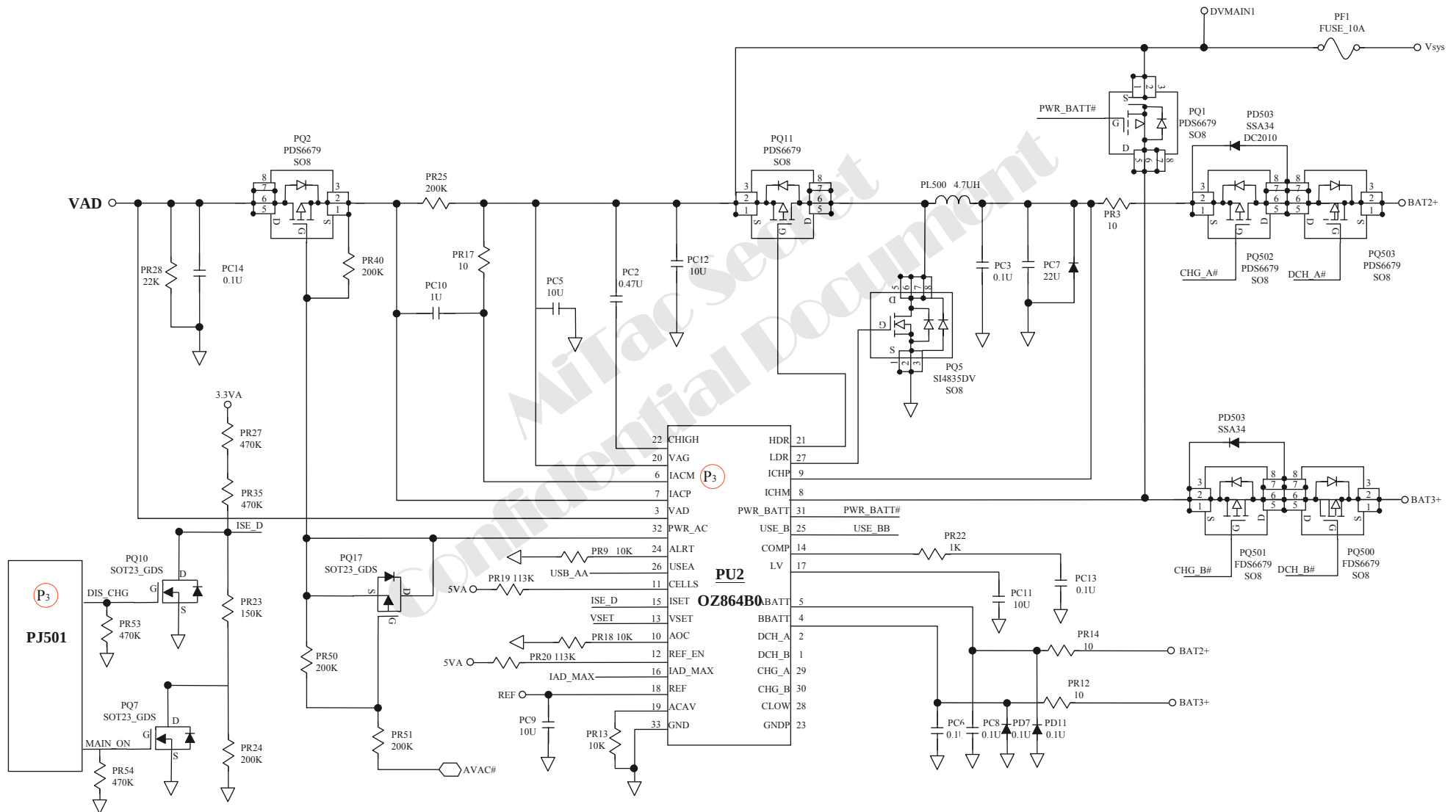
- VAC** (Pin 9): Connected to the VAD input.
- HDR** (Pin 10): Connected to the HDR input.
- CHIGH** (Pin 11): Connected to the CHIGH input.
- ACAP** (Pin 12): Connected to the ACAP input.
- ICHP** (Pin 13): Connected to the ICHP input.
- ICHM** (Pin 14): Connected to the ICHM input.
- IACM** (Pin 15): Connected to the IACM input.
- ISET** (Pin 16): Connected to the ISET input.
- REF** (Pin 8): Connected to the REF input.
- LV** (Pin 7): Connected to the LV input.
- GND** (Pin 6): Connected to ground.
- COMP** (Pin 5): Connected to the COMP input.
- VSET** (Pin 4): Connected to the VSET input.
- ICHG** (Pin 3): Connected to the ICHG input.
- CELLS** (Pin 2): Connected to the CELLS input.
- ISET** (Pin 1): Connected to the ISET input.

The diagram includes various components such as resistors (PR), capacitors (PC), diodes (PD), and transistors (PQ). A large watermark 'Confidential Document' is overlaid on the diagram.

A790 N/B Maintenance

8.1 No Power-4

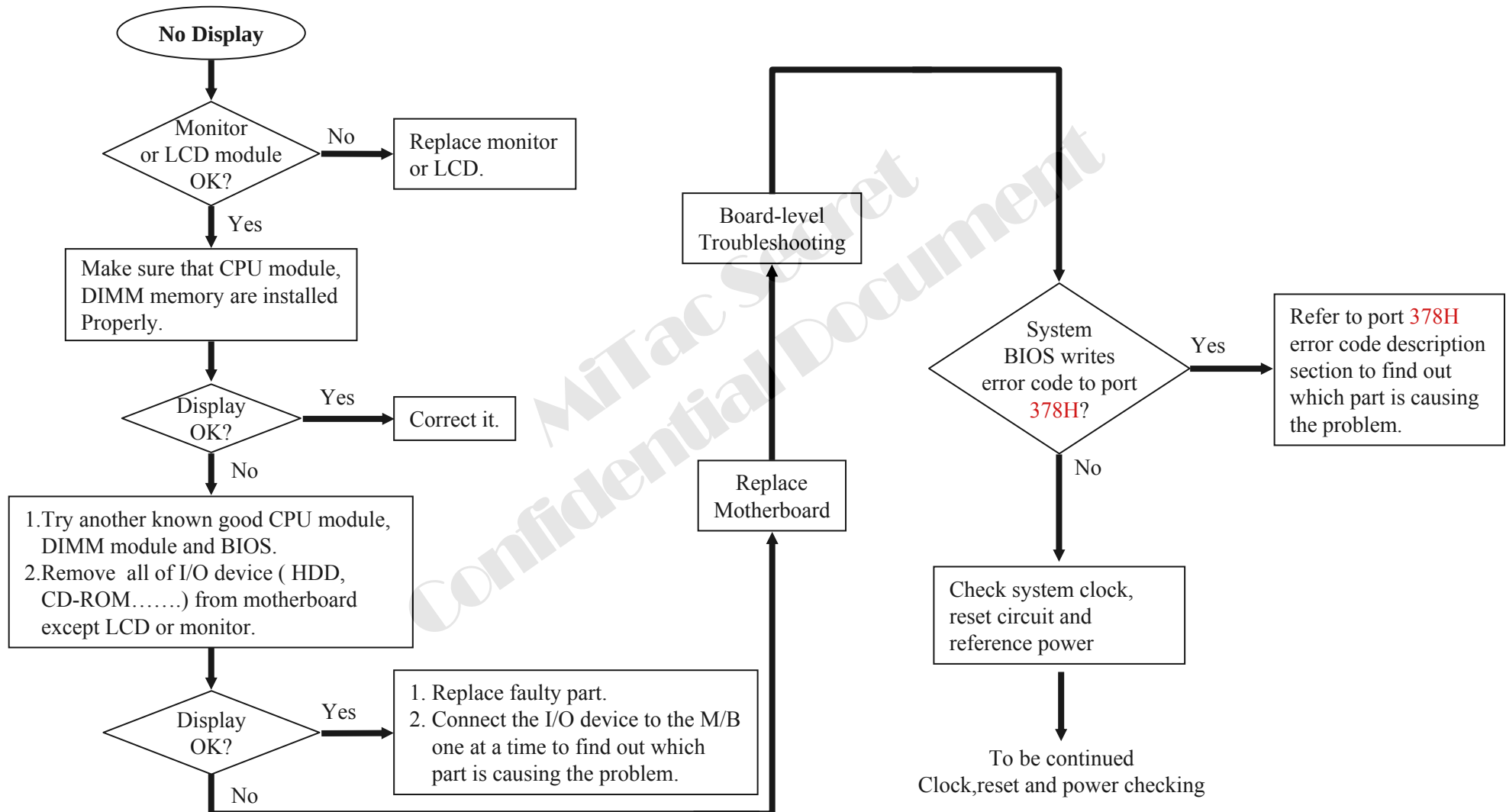
When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



A790 N/B Maintenance

8.2 No Display-1

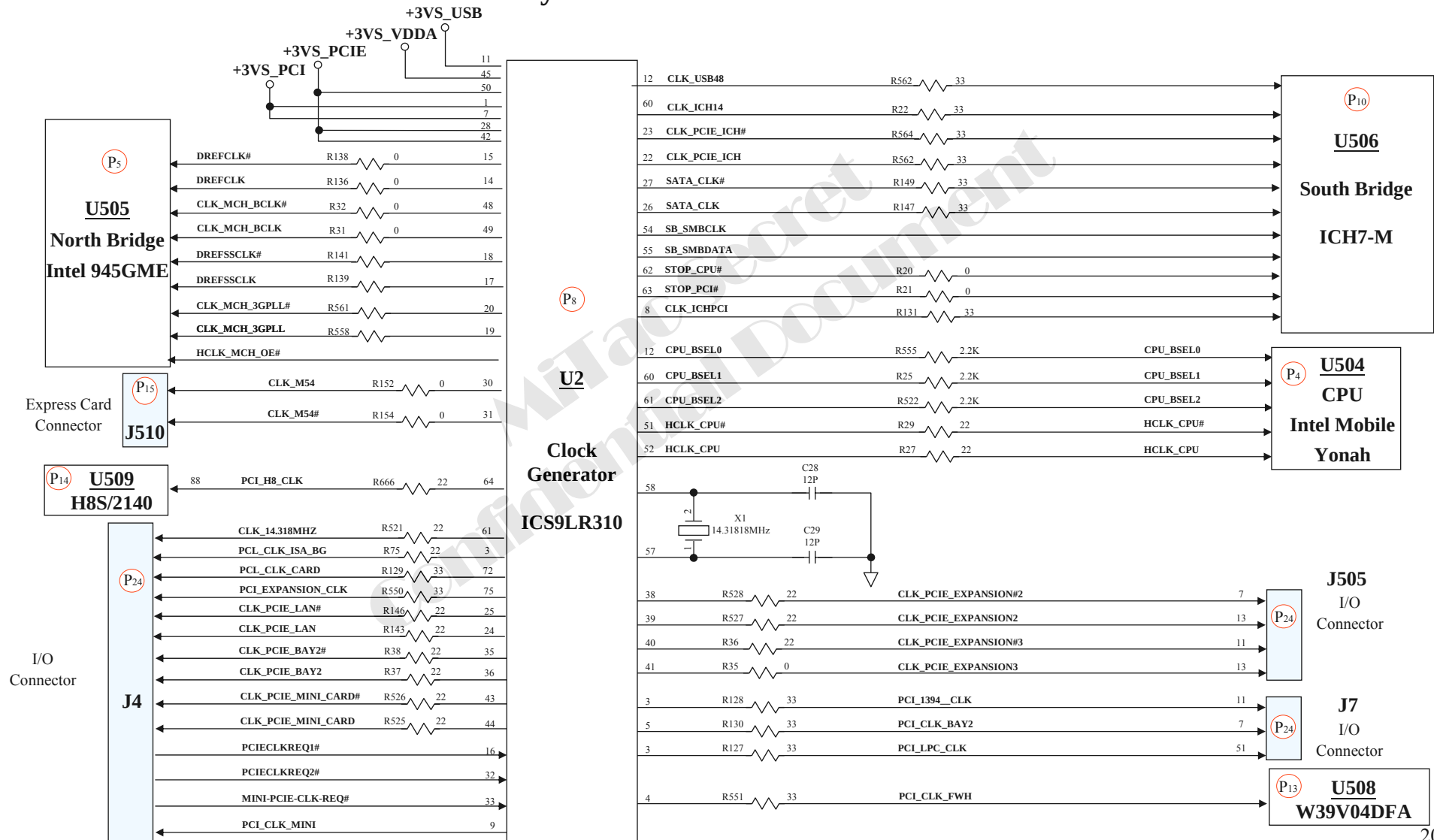
There is no display on both LCD and VGA monitor after power on although the LCD and monitor is known-good.



A790 N/B Maintenance

8.2 No Display-2

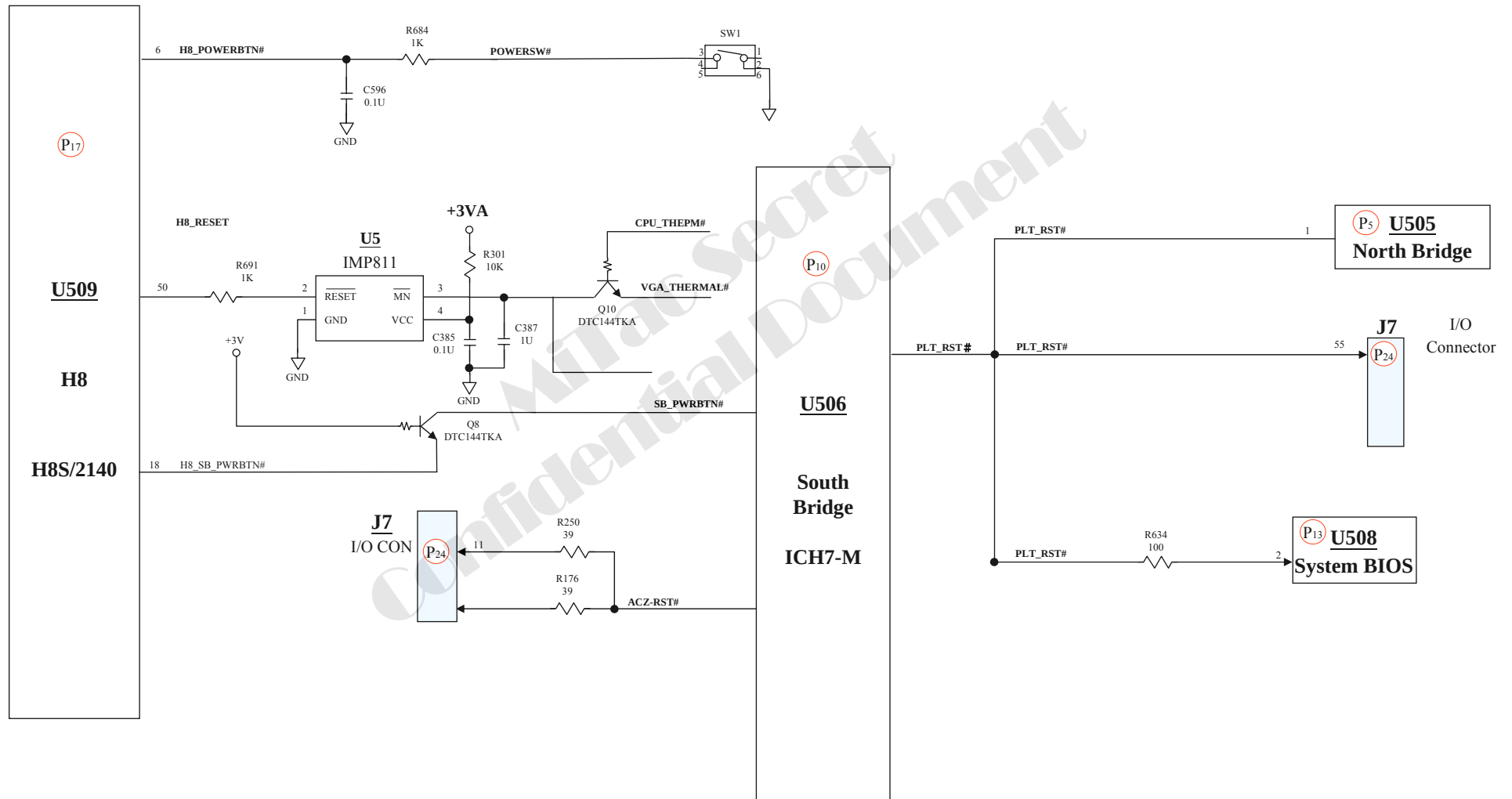
***** System Clock Check *****



A790 N/B Maintenance

8.2 No Display-3

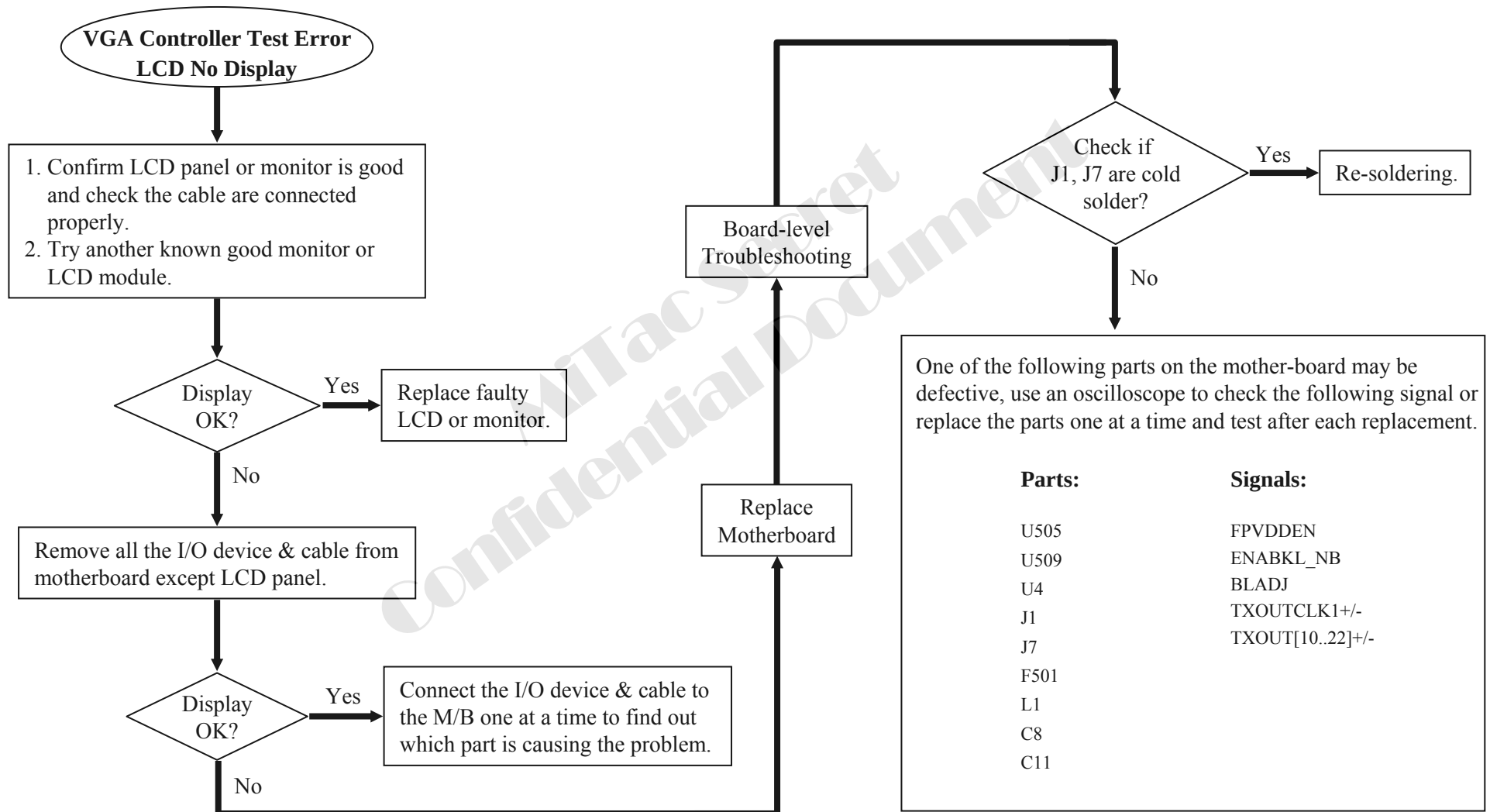
***** Power Good & Reset Circuit Check *****



A790 N/B Maintenance

8.3 Graphics Controller Test Error LCD No Display-1

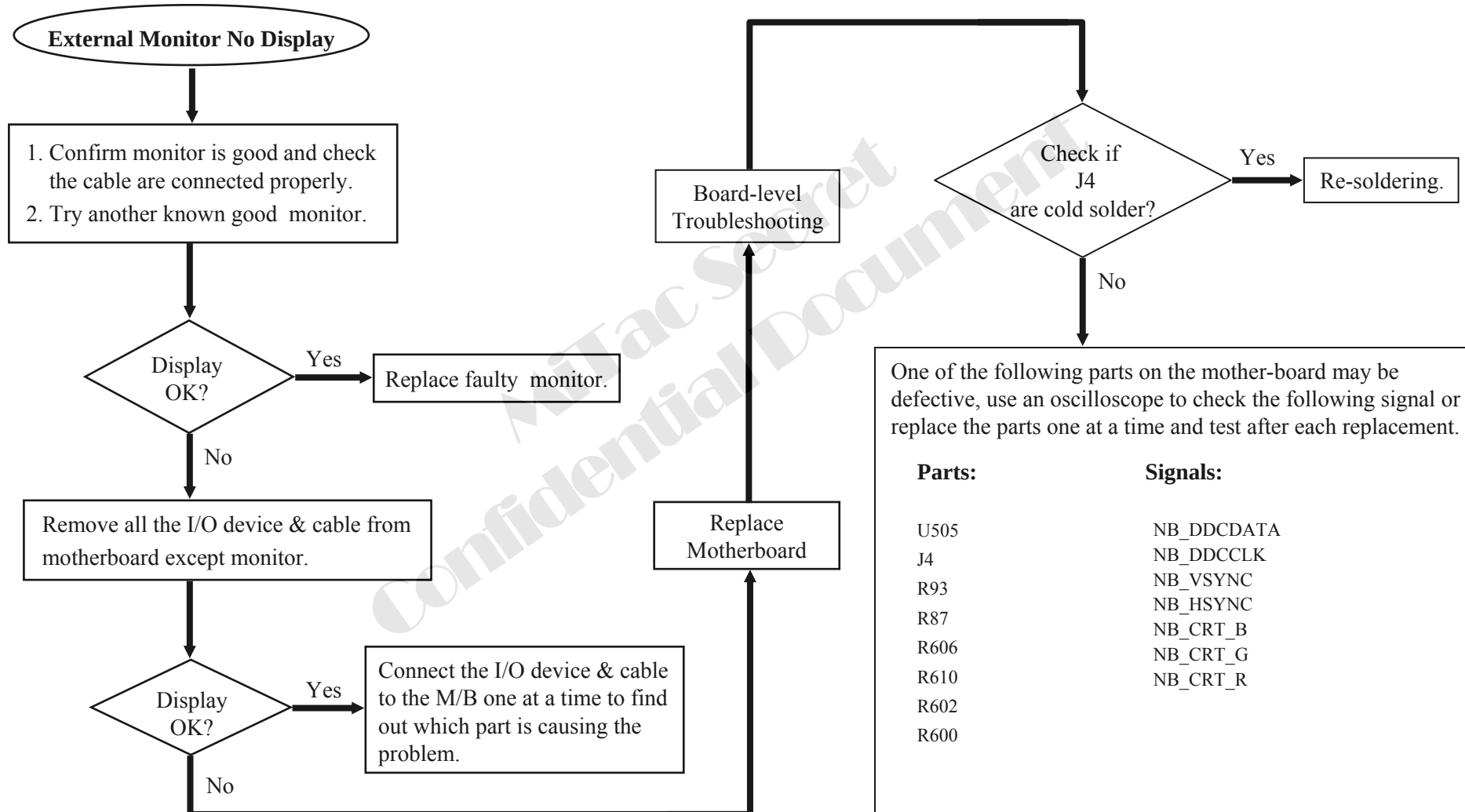
There is no display or picture abnormal on LCD although power-on-self-test is passed.



A790 N/B Maintenance

8.4 External Monitor No Display-1

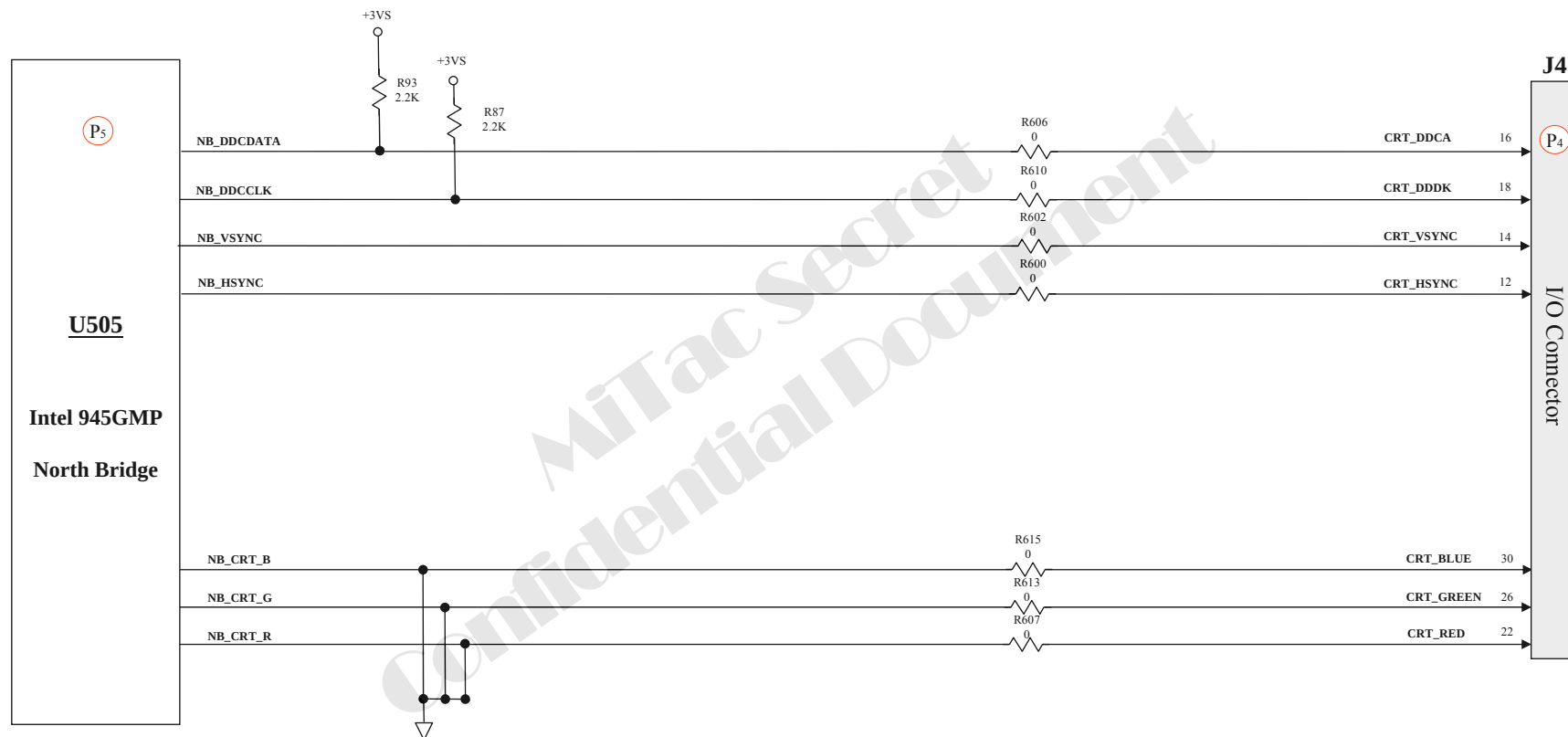
There is no display or picture abnormal on CRT/DVI monitor, but it is OK for LCD.



A790 N/B Maintenance

8.4 External Monitor No Display-2

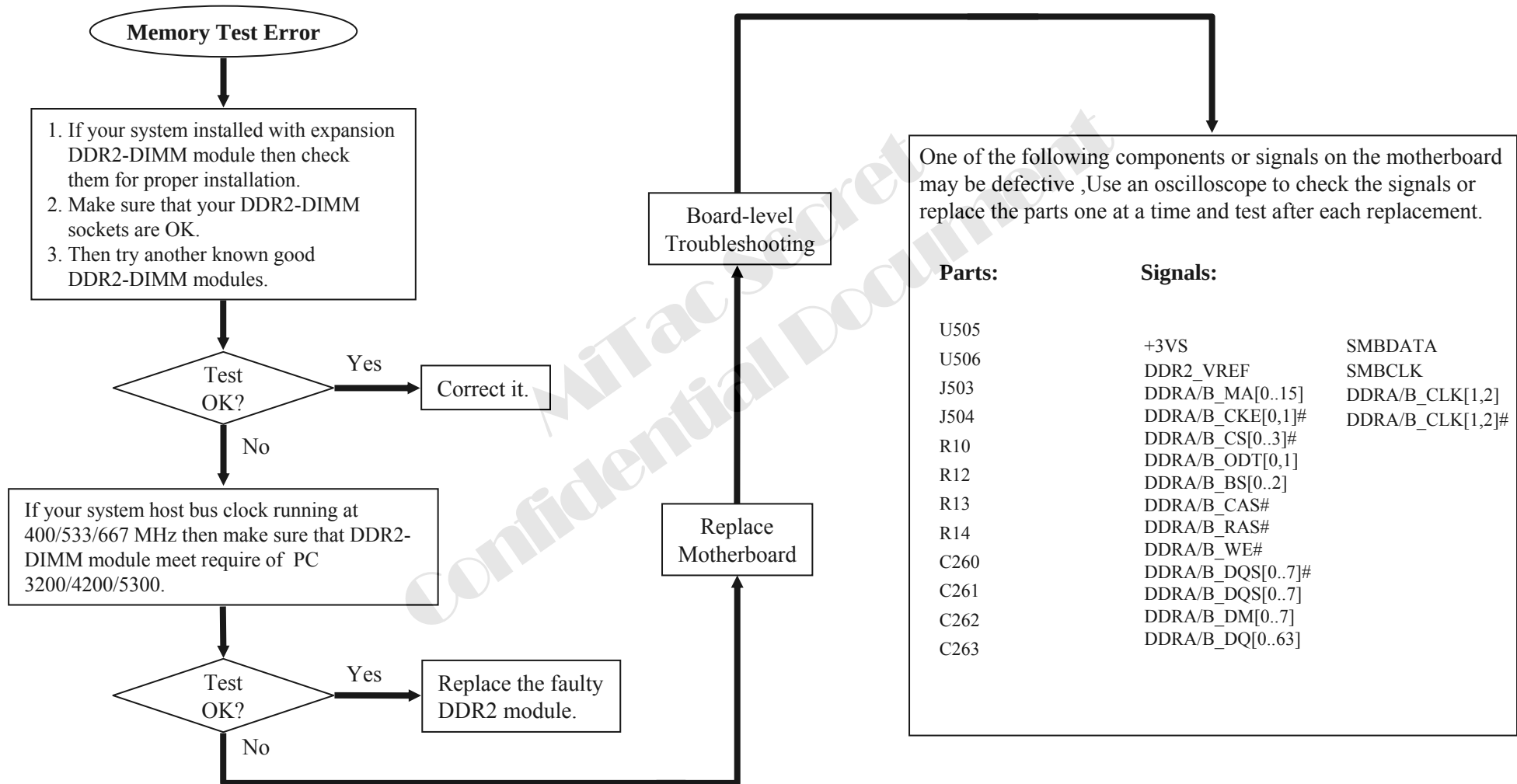
There is no display or picture abnormal on CRT monitor, but it is OK for LCD.



A790 N/B Maintenance

8.5 Memory Test Error-1

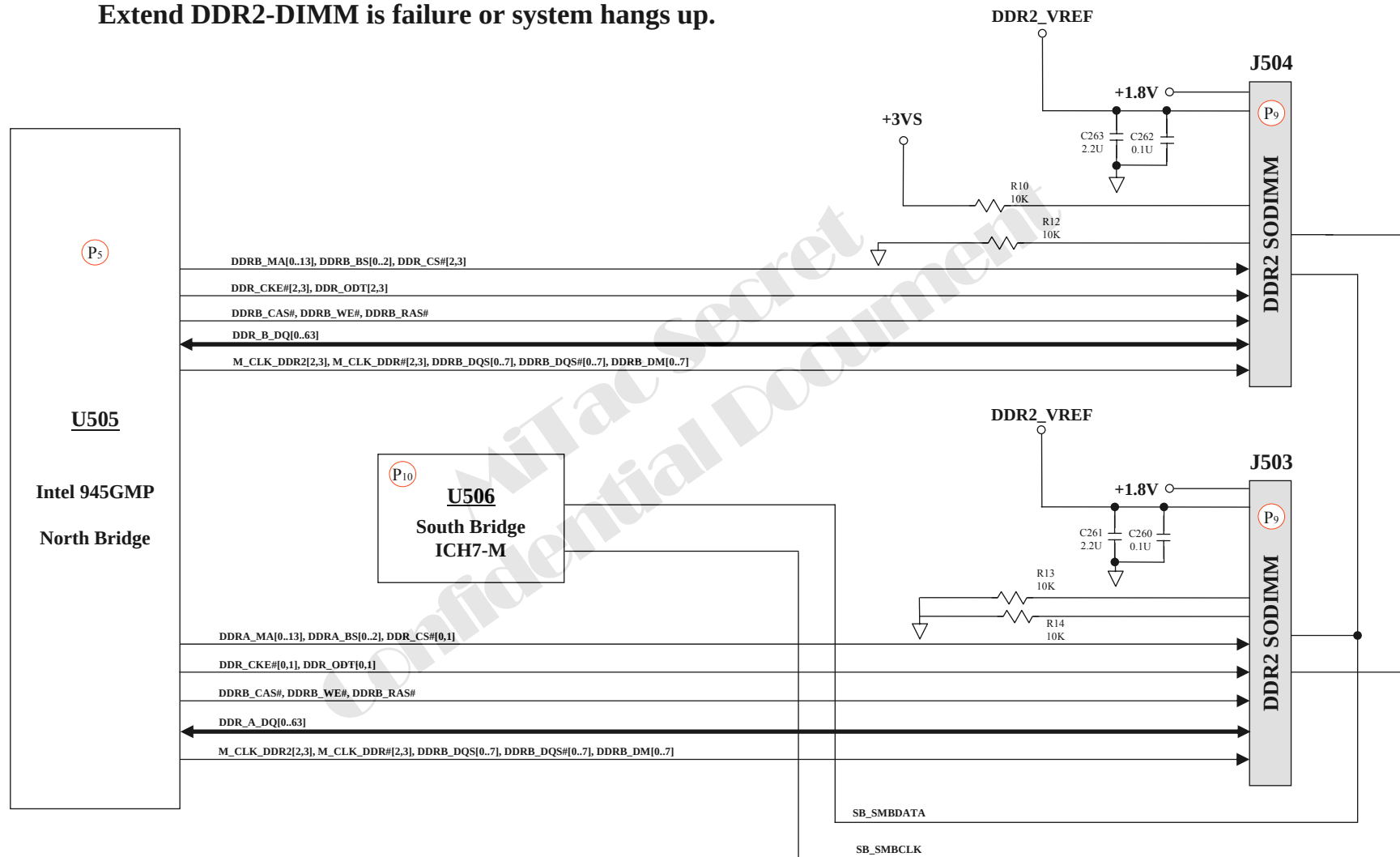
Extend DDR2-DIMM is failure or system hangs up.



A790 N/B Maintenance

8.5 Memory Test Error-2

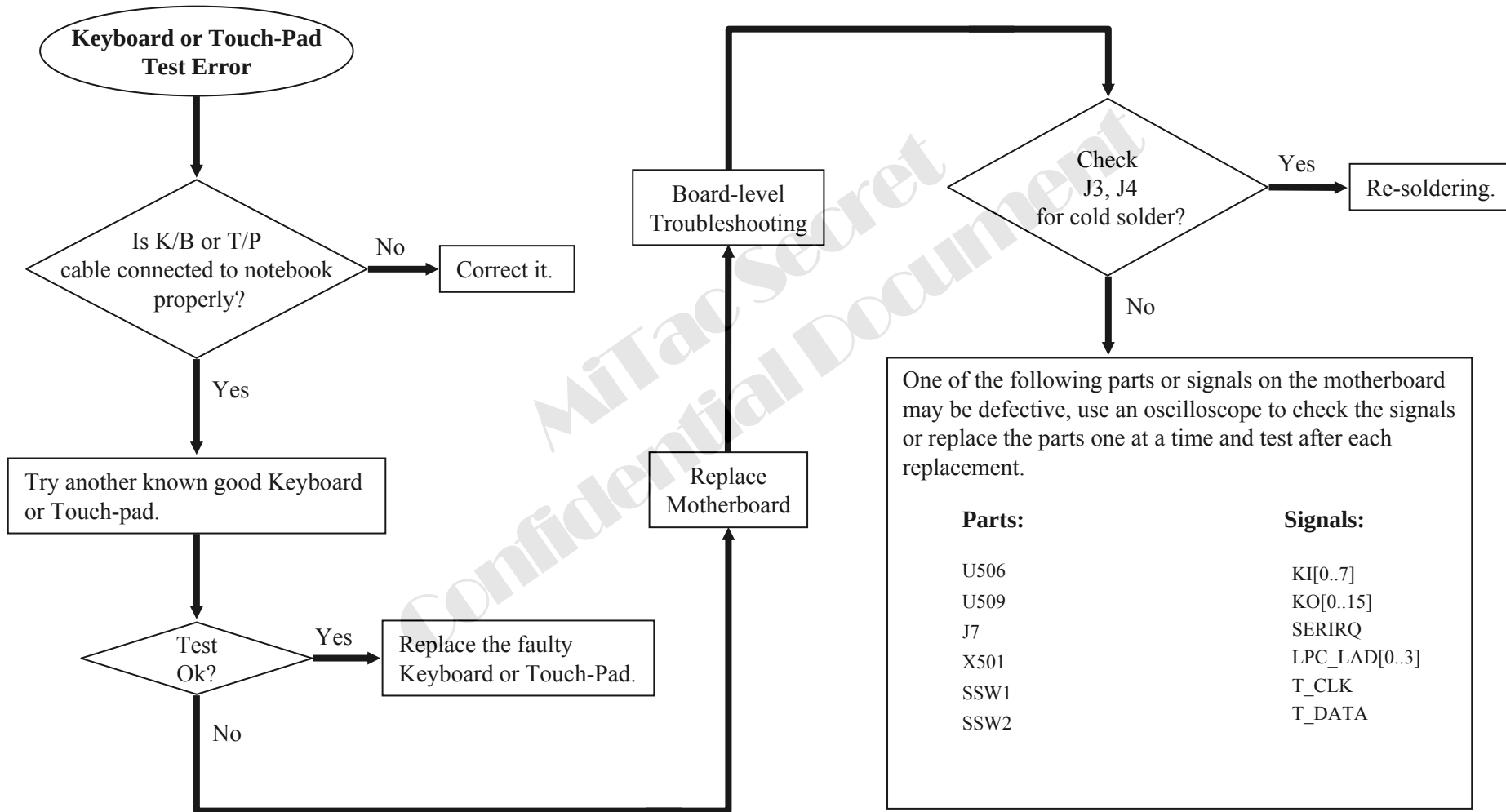
Extend DDR2-DIMM is failure or system hangs up.



A790 N/B Maintenance

8.6 Keyboard (K/B) or Touch-Pad (T/P) Test Error-1

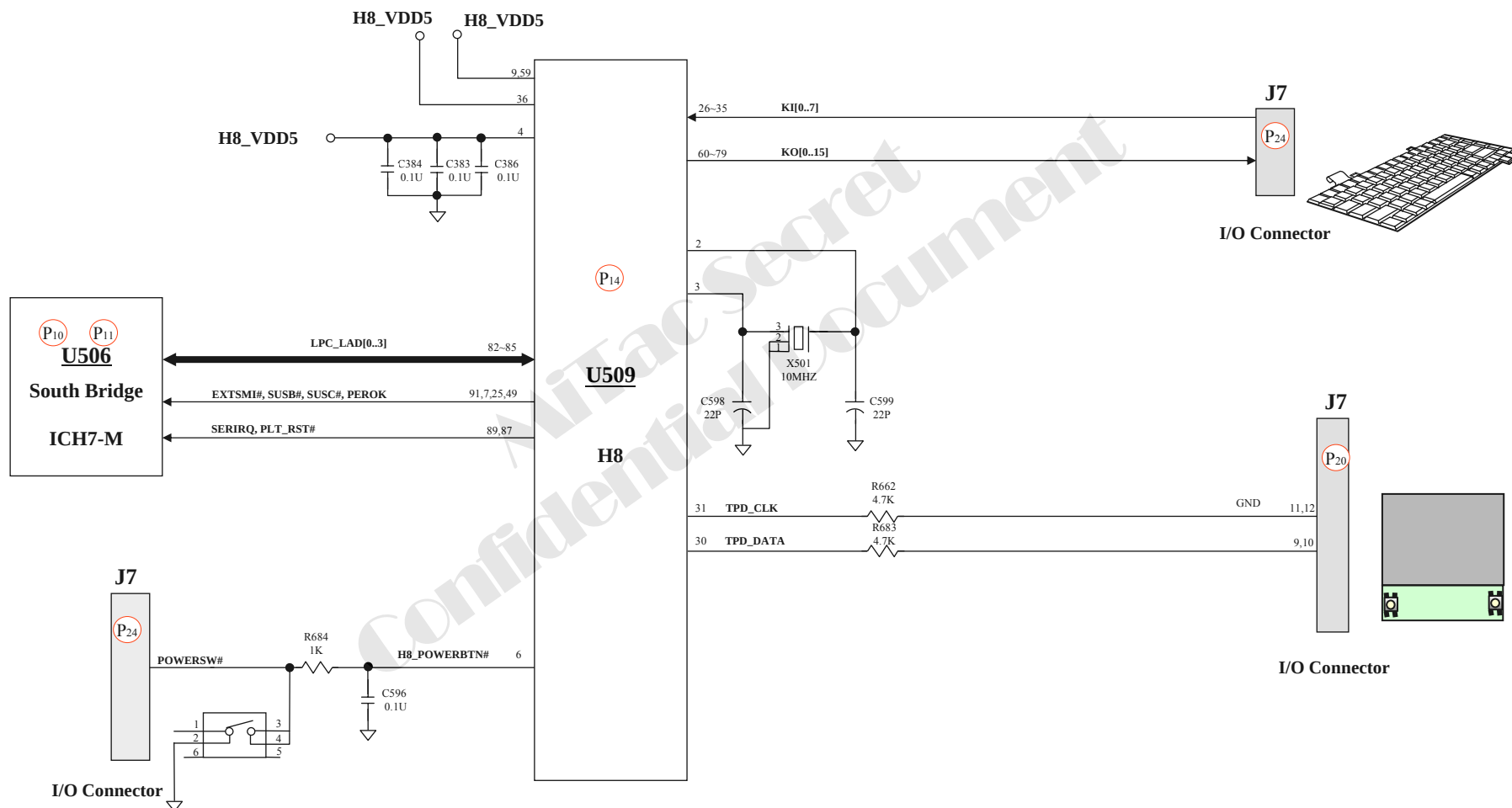
Error message of keyboard or touch-pad failure is shown or any key does not work.



A790 N/B Maintenance

8.6 Keyboard (K/B) or Touch-Pad (T/P) Test Error-2

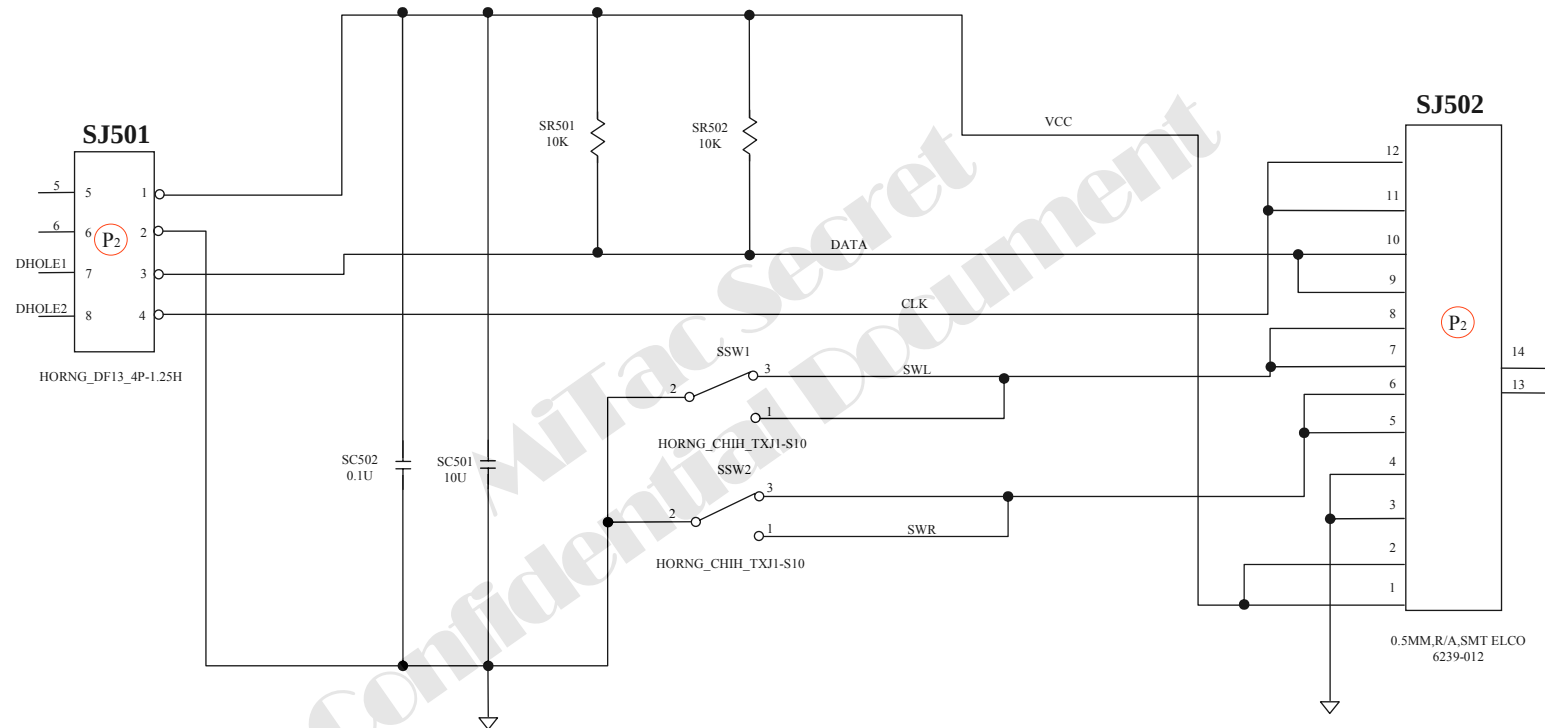
Error message of keyboard or touch-pad failure is shown or any key does not work.



A790 N/B Maintenance

8.6 Keyboard (K/B) or Touch-Pad (T/P) Test Error-3

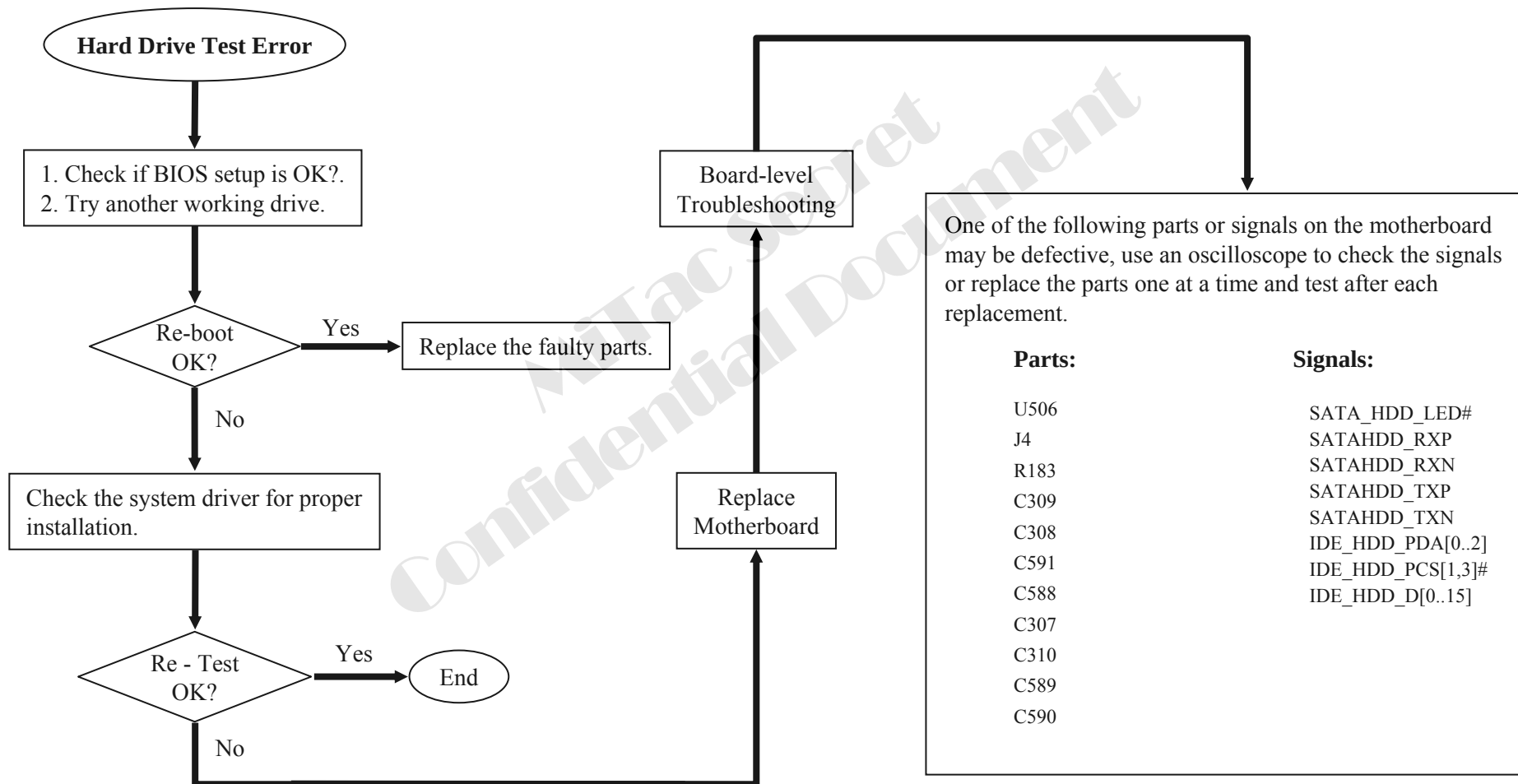
Error message of keyboard or touch-pad failure is shown or any key does not work.



A790 N/B Maintenance

8.7 Hard Drive Test Error-1

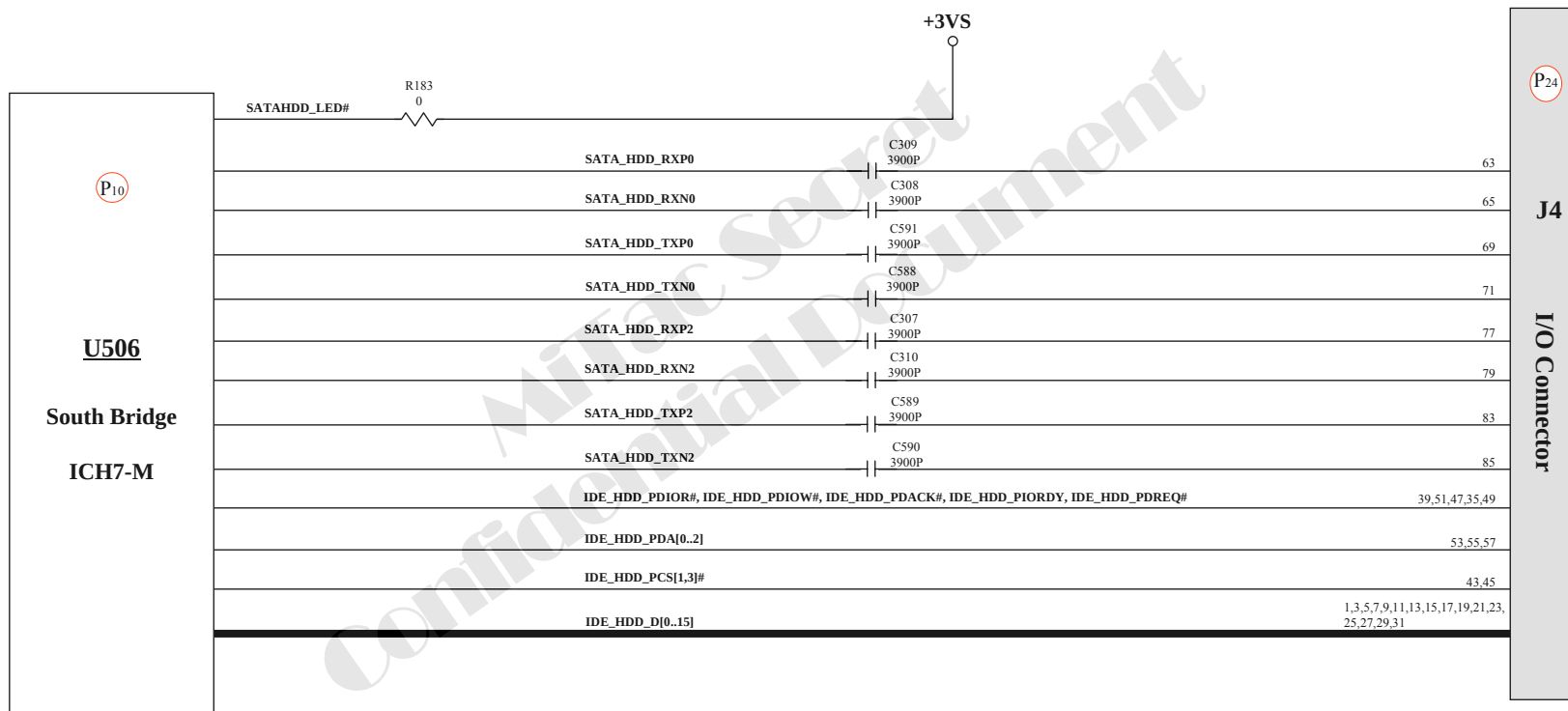
Either an error message is shown, or the drive motor spins non-stop, while reading data from or writing data to hard disk.



A790 N/B Maintenance

8.7 Hard Drive Test Error-2

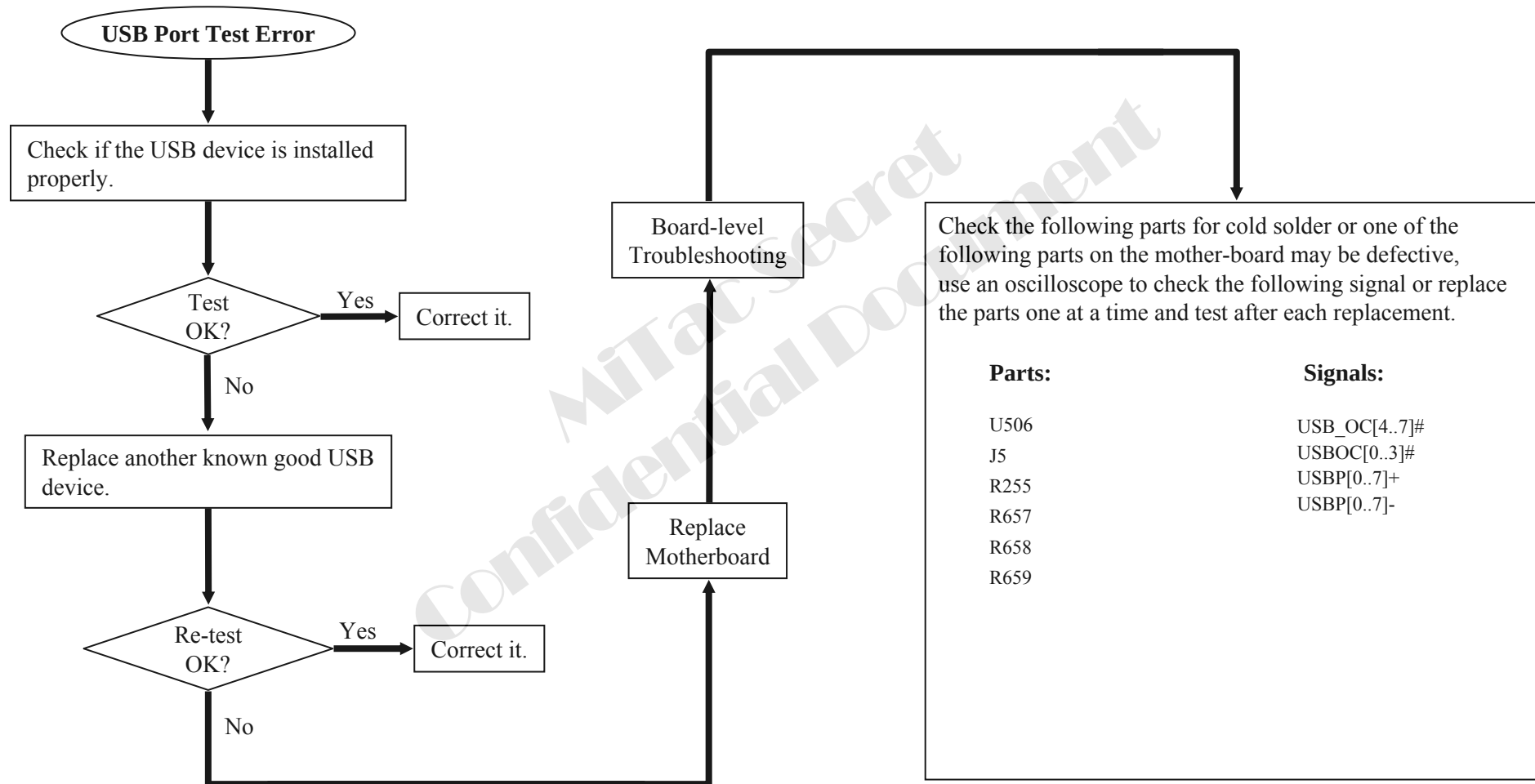
Either an error message is shown, or the drive motor spins non-stop, while reading data from or writing data to hard disk.



A790 N/B Maintenance

8.8 USB Port Test Error-1

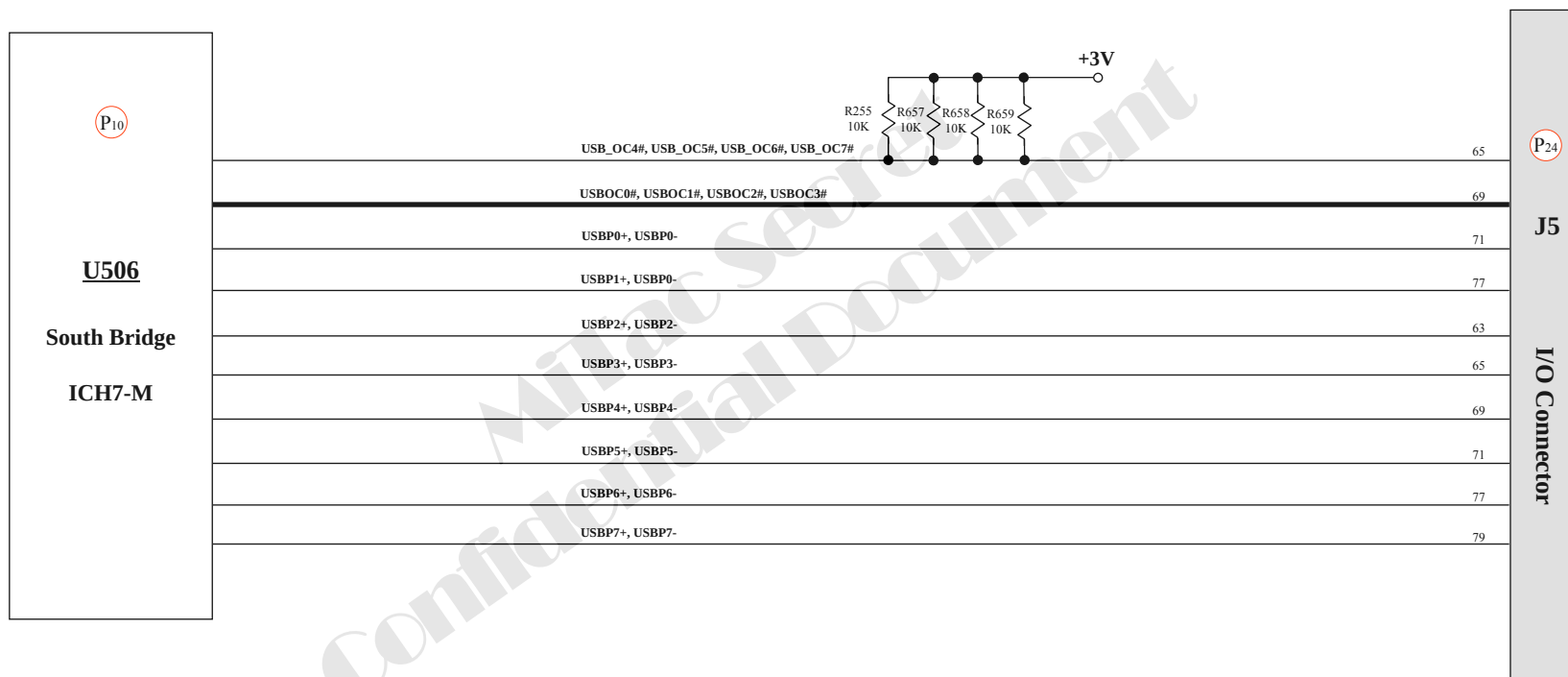
An error occurs when a USB I/O device is installed.



A790 N/B Maintenance

8.8 USB Port Test Error-2

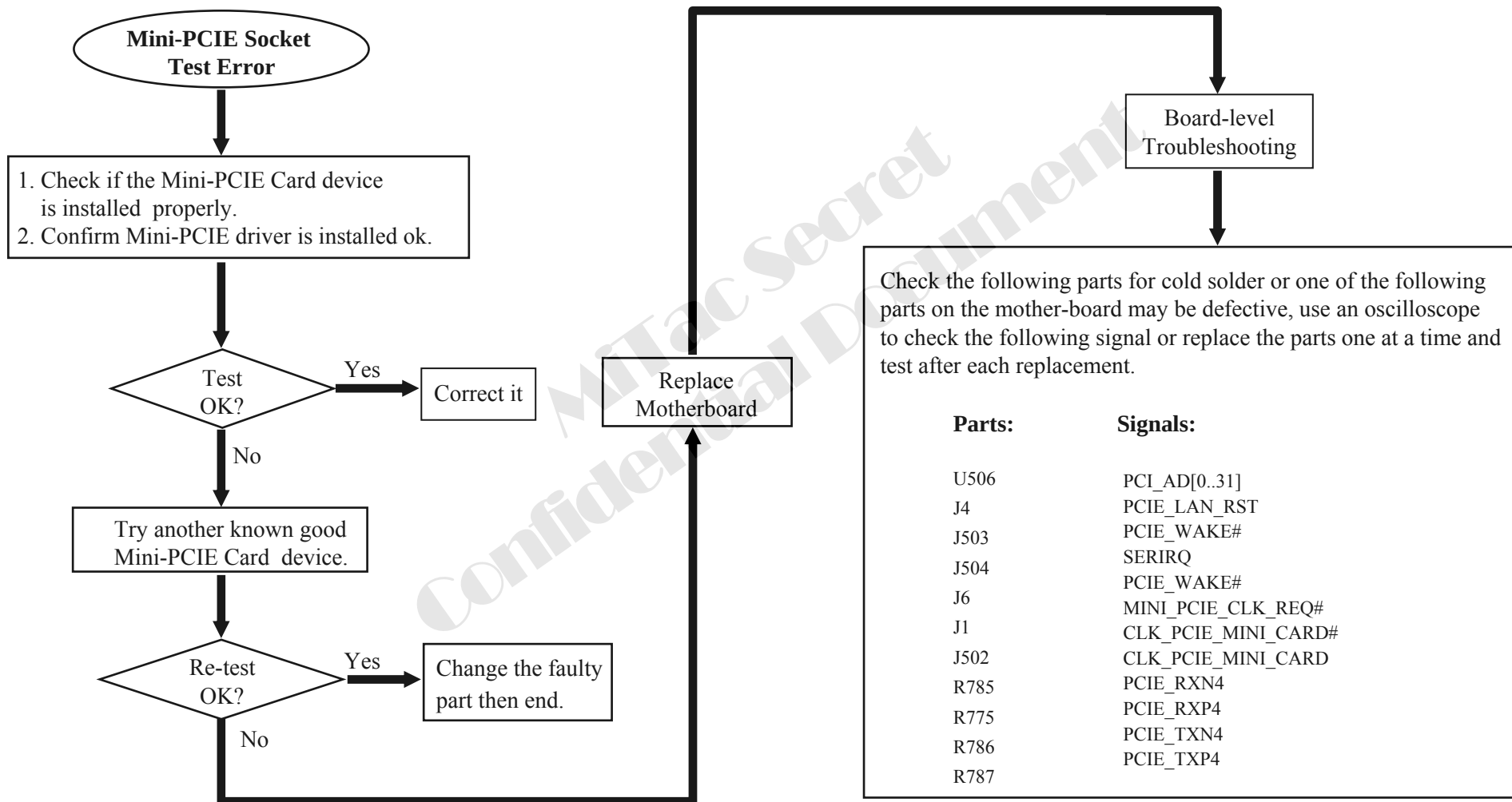
An error occurs when a USB I/O device is installed.



A790 N/B Maintenance

8.9 Mini-PCIE Socket Test Error-1

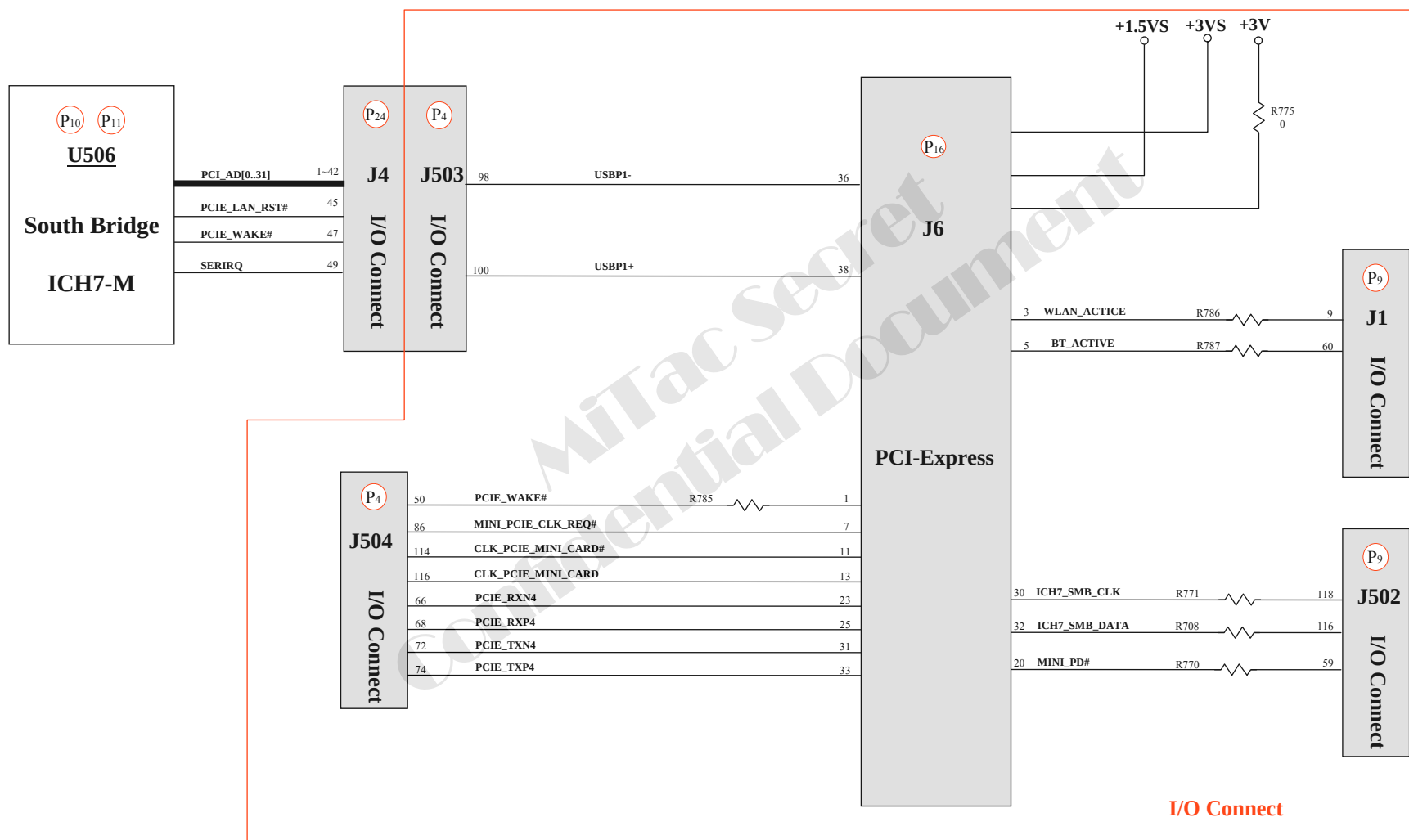
An error occurs when a Mini-PCIE Card device is installed.



A790 N/B Maintenance

8.9 Mini-PCIE Socket Test Error-2

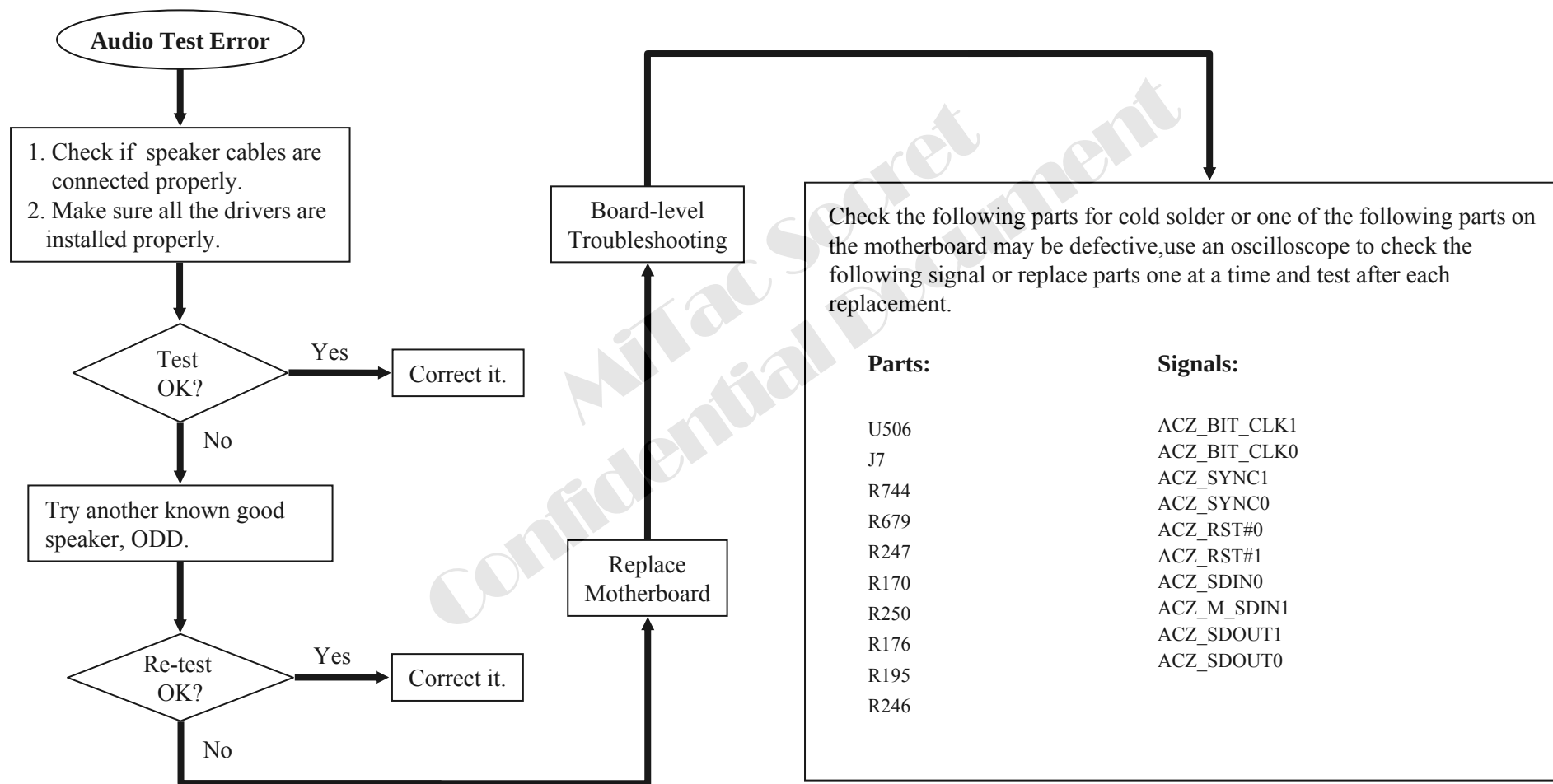
An error occurs when a Wireless LAN Card device is installed.



A790 N/B Maintenance

8.10 Audio Test Error-1

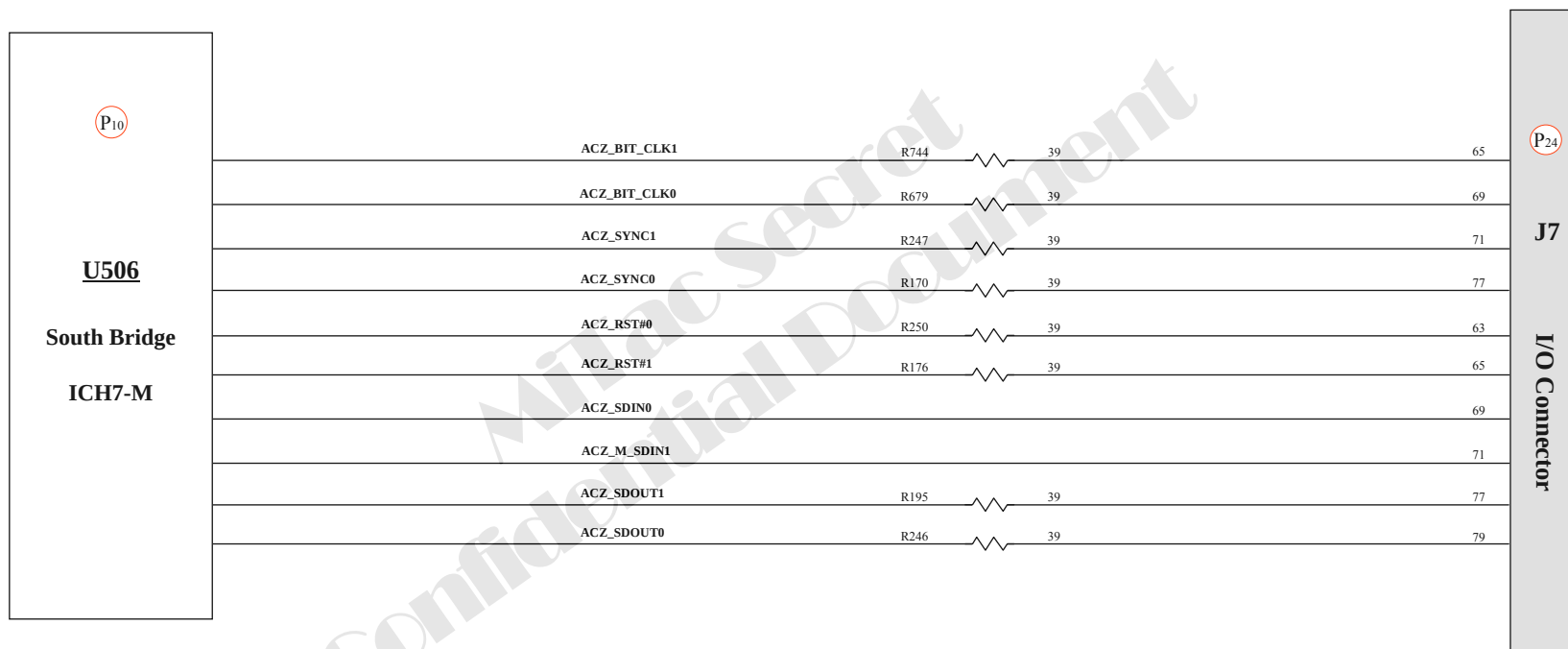
No sound from speaker after audio driver is installed.



A790 N/B Maintenance

8.10 Audio Test Error-2

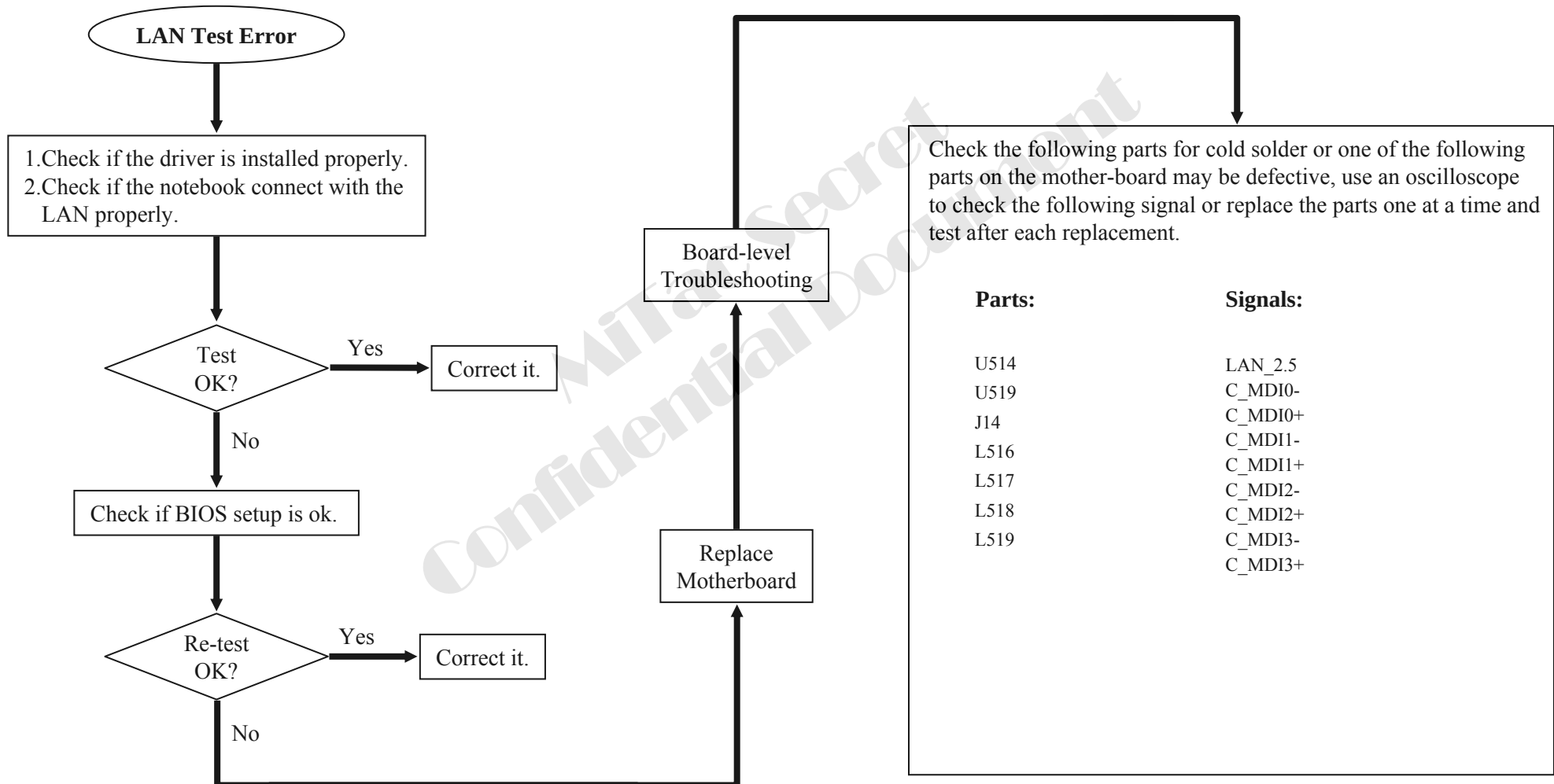
No sound from speaker after audio driver is installed.



A790 N/B Maintenance

8.11 LAN Test Error-1

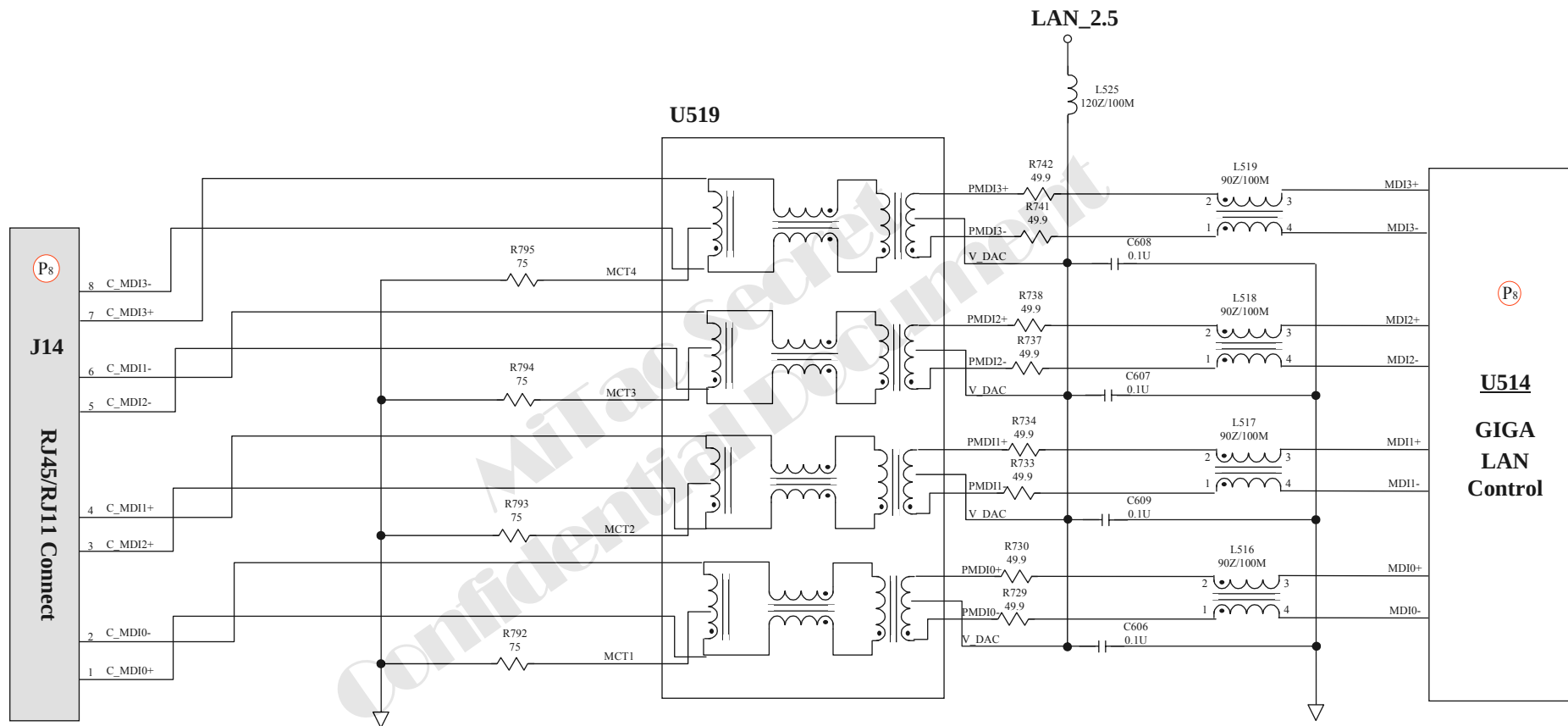
An error occurs when a LAN device is installed.



A790 N/B Maintenance

8.11 LAN Test Error-2

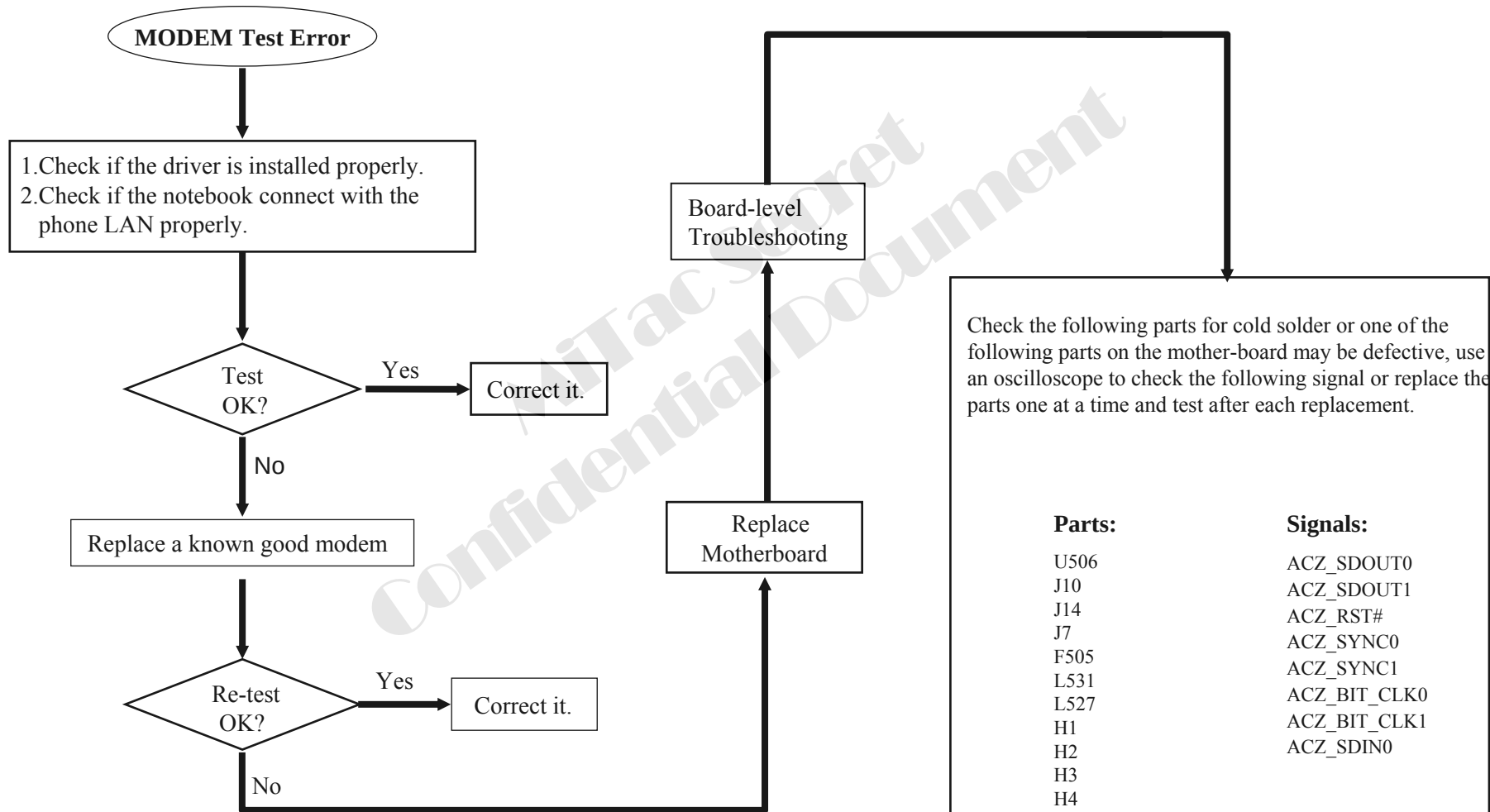
An error occurs when a LAN device is installed.



A790 N/B Maintenance

8.12 Modem Test Error

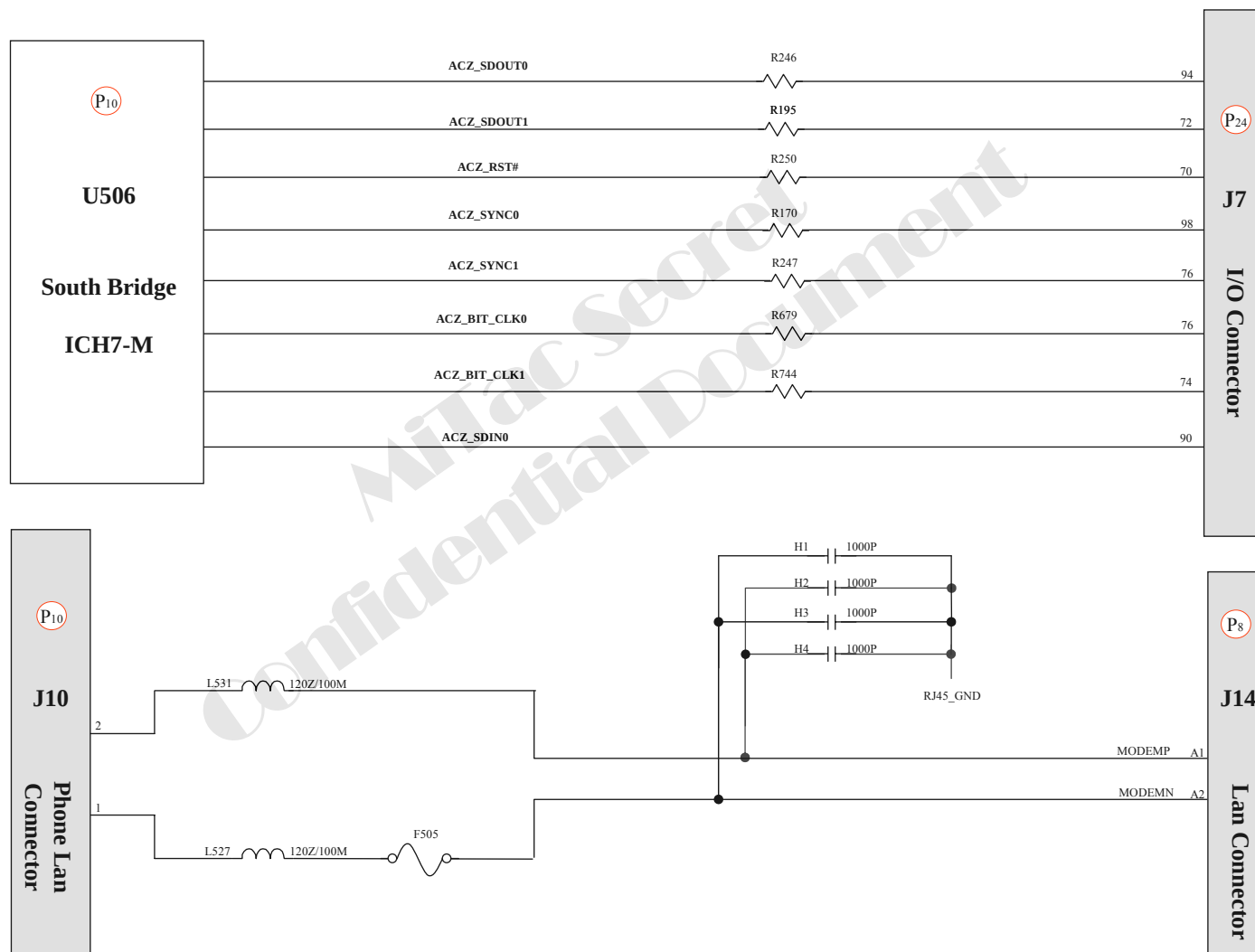
An error occurs when run the modem.



A790 N/B Maintenance

8.12 Modem Test Error

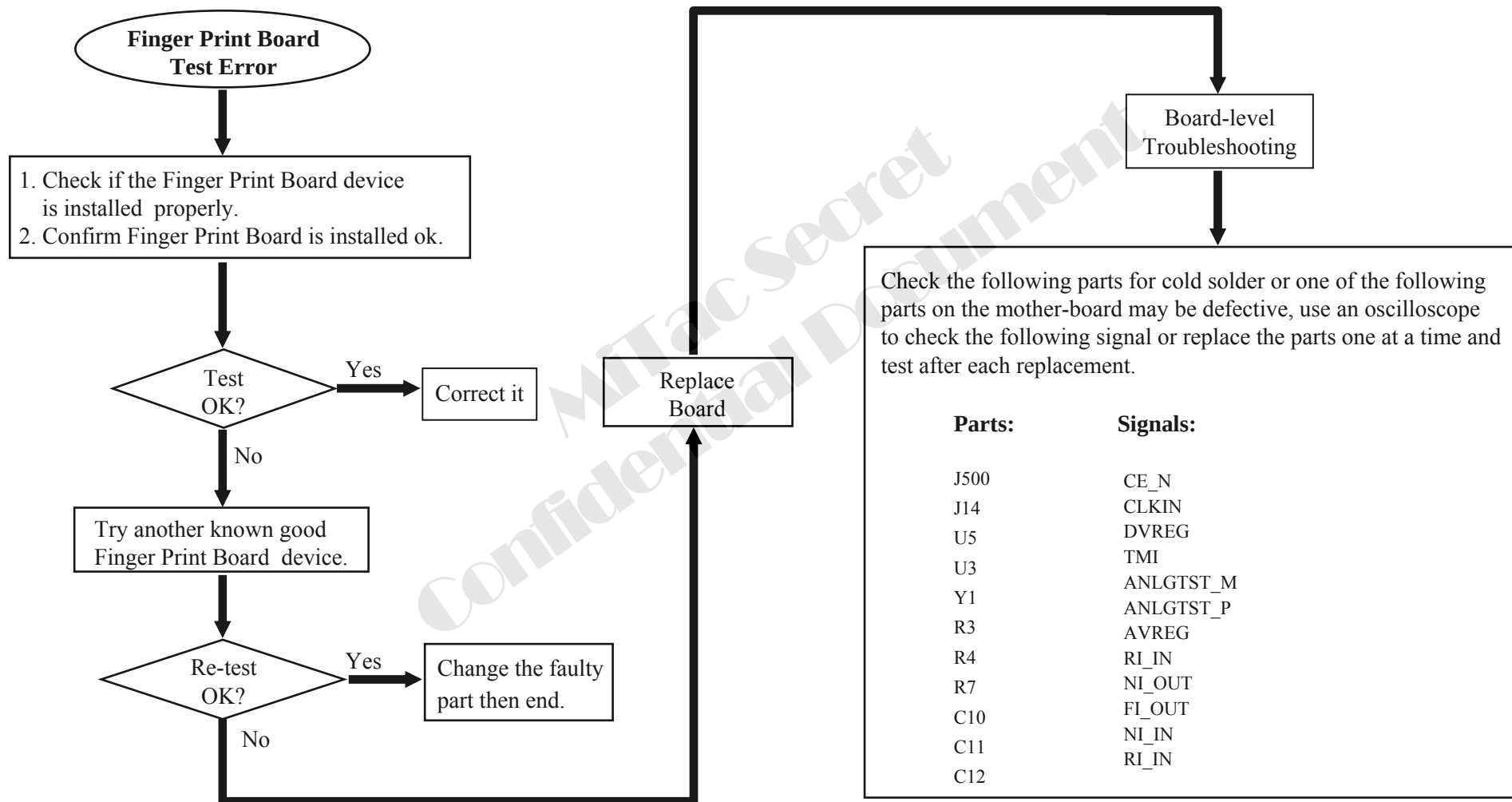
An error occurs when run the modem.



A790 N/B Maintenance

8.13 Finger Print Board Test Error

An error occurs when a Mini-PCIE Card device is installed.



A790 N/B Maintenance

9. Spare Parts List - 1

Part Number	Deacription	Location(S)
791901190001	NB0;A790-7,S33,USA1,15-TE-5D5	
791911182009	TF041-S/W ASSY;NULL,(0)DUMMY	
791911190010	TF041-LCD ASSY;A790-(7,S33)TO	
345118200002	TF041-GASKET;LCD 12.1",A-SERI	
413000020645	TF041-LCD;LTD121EC5S,TFT,12.1	
791941190001	TF041-HOUSING ASSY;LCD,A790-7	
412119000001	TF041-INVERTER ASSY;14.1",12.	
221800920001	TF041-CARTON;380MM*320MM*150M	
226800900001	TF041-SPONGE;370MM*310MM*10MM	
344801200003	TF041-BOX;PVC,T=0.5MM,PWR	
346119000001	TF041-INSULATOR;8B35,A790 INV	
365350000009	LF-SOLDER WIRE;SN96.5/AG3.0/C	
411115000128	TF041-PWA;PWA-DA-1A08-I04(L)	
271071000312	TF041-TH-RES;0 ,1/16W,5% ,	R5
271071103310	TF041-TH-RES;10K ,1/16W,5% ,	R4
271071104108	TF041-TH-RES;100K ,1/16W,1% ,	R8
271071105312	TF041-TH-RES;1M ,1/16W,5% ,	R12
271071183103	TF041-TH-RES;18K ,1/16W,1% ,	R20
271071224305	TF041-TH-RES;220K ,1/16W,5% ,	R21
271071395101	TF041-TH-RES;3.9M ,1/16W,1% ,	R9
272003105402	TF041-TH-CAP;1U ,CR,25V ,10	C7
272010181302	TF041-TH-CAP;180P,2KV,5%,1206	C3
272030000301	TF041-TH-CAP;15P,3KV,5%,1808,	C4
272071105411	TF041-TH-CAP;1U ,10V ,10%,060	C13
272072105403	TF041-TH-CAP;0.1U ,CR,16V,10	C15,C8

Part Number	Deacription	Location(S)
272072224405	TF041-TH-CAP;0.22U ,16V ,10%,	C9
272072473409	TF041-TH-CAP;0.047U,16V ,10%,	C14
272073105404	TF041-TH-CAP;1UF ,25V,10%,06	C2
272073223407	TF041-TH-CAP;.022U,CR,25V ,10	C16
272073332405	TF041-TH-CAP;3300P,CR,25V ,10	C12
272075183402	TF041-TH-CAP;0.018U,50V ,10%	C6
288100099015	TF041-TH-DIODE;BAV99,70V,450M	D1,D2
288206602003	TF041-TH-TRANS;AO6602L,N&P-MO	U1,U3
291000020229	TF041-TH-CON;HDR,MA,2P*1,3.5M	CN2
291000910802	TF041-CON;HDR,MA,8P,1.25,R/A,	CN1
316115000042	TF041-PCB;PWA-DA-1A08-I04(L)	R0B
286009910005	TF041-TH-IC;OZ9910ISN,CCFL CT	U2
271071303103	TF041-TH-RES;30K,1/16W,1%,060	R1
271071333102	TF041-TH-RES;33K ,1/16W,1% ,	R7
271071564304	TF041-TH-RES;560K ,1/16W,5% ,	R6
271071823106	TF041-TH-RES;82K,1/16W,1%,060	R2
272013106504	TF041-TH-CAP;10U,25V,+/-20%,1	C1
272075181308	TF041-TH-CAP;180P ,50V ,5% ,0	C10
273001050279	TF041-TH-XFMR;CI8.5,20T/2000T	T1
295000010248	TF041-TH-FUSE;FAST,1.5A,63VDC	F1
272073180406	TF041-TH-CAP;18P,CR,50V,5%,06	C11
271071591103	TF041-TH-RES;590,1/16W,1%,060	R15
271071124116	TF041-TH-RES;120K ,1/16W,1% ,	R14
242804400010	TF041-TH-LABEL;BAR CODE,20*5,	
361200003204	TF041-SOLDER PASTE;PF606-P;FO	

A790 N/B Maintenance

9. Spare Parts List - 2

Part Number	Deacription	Location(S)
796119070014	TF041-DUO-PAK,DP-420,OFF-WHIT	
346115000007	TF041-THERMAL PAD;SR800A,L33W	
796119011003	TF041-HINGE;ROT SHFT,A-790	
796119061004	TF041-RUBBER SPONGE;85*15*3t,	
796119052007	TF041-WASHER;LCD,BUMP,A-790	
796119061001	TF041-SPONGE; 244*8*3.5t, A-7	
796119062030	TF041-RUBBER;LCD,BUMP 12.1",A	
797425206000	TF041-WASH;M3,SPR,SUS,PSV	
796119061028	TF041-PORON;27*11*1.5 ,A-790	
796119061029	TF041-PORON;40*11*1.5,A-790	
796119061030	TF041-PORON;31*11*1.5 ,A-790	
796119061031	TF041-PORON;6.6*11*1.5,A-790	
796119060043	TF041-RUBBER;200*6*1.2T,A790	
796119060044	TF041-RUBBER;200*6*2T,A790	
796119071004	TF041-GASKET;ψ1.8,A790	
796119061053	TF041-Rubber;10*10*10,A790	
796119061054	TF041-Rubber;10*10*2.5,A790	
796115050087	TF041-FIXTURE;INVER PCB CABLE	
796119070027	TF041-SCR;M3L8,RND,SUS,PSV,6M	
796119002019	TF041-BASE;WCDMA ANTENNA,12.1	
796119060056	TF041-RUBBER;LCD BUMPER-R,WCD	
796119060057	TF041-RUBBER;LCD BUMPER-L,WCD	
791941190091	TF041-COVER ASSY;KBD,A790-7,T	
411119000007	TF041-TH-PWA;PWA-A790,LED&SW	
411119000008	TF041-TH-PWA;PWA-A790,LED&SW	

Part Number	Deacription	Location(S)
411119000009	TF041-TH-PWA;PWA-A790,LED&SW	
297212000006	TF041-TH-RELAY;REED,200V,0.5A	S2
294011200536	TF041-TH-LED;YEL/GRN,H1.1,L3.	D19,D20,D21
272072102503	TF041-TH-CAP;1000P,16V ,20%,0	C605
291000410208	TF041-TL-CON;WFR,MA,2P,1.25,S	J507
291000411504	TF041-TL-CON;WFR,MA,15P,1.25V	J508
316119000003	TF041-TH-PCB;PWA-A790,LED&SW	R01
242600000572	TF041-LABEL;4*3MM,HI-TEMP,260	
297040100041	TF041-TH-SW;PUSH BUTTON,H=4.3	S1
291000010629	TF041-TH-CON;HDR,MA,6P,1.25mm	J509
291000151007	TF041-TH-CON;FFC/FPC R/A P=0.	J510
294011200388	TF041-TH-LED;YEL,2.1V/20MA,SM	D15,D16,D17,D18
271071549114	TF041-TH-RES;549 ,1/16W,1% ,	R723,R724,R725,R726,R727R728
422118200022	TF041-TH-CABLE ASSY;KEYBOARD	
796119001000	TF041-SWITCH COMP;TRACK PAD,A	
796119051005	TF041-BRKT;TRACK PAD,A-790	
796119051014	TF041-LED WINDOW;A-790	
796119061017	TF041-BUTTON;POWER,A-790	
422118200038	TF041-TH-CABLE ASSY;TOSHIBA 1	
422119000016	TF041-CABLE ASSY;I/O TO INVR	
791941190142	TF041-HOUSING ASSY;NON-COMMON	
796119000001	TF041-RUBBER HINGE,LF;A-790	
796119000002	TF041-RUBBER HINGE,RH;A-790	
796119061019	TF041-COVER;SCREW,A-790	
796119060030	TF041-RUBBER;PLUG,LCD BUMPER,	

A790 N/B Maintenance

9. Spare Parts List - 3

Part Number	Deacription	Location(S)
796119000004	TF041-RUBBER BUMPER;A-790	
796119012001	TF041-HOLDER;SCREW,A-790	
796119030001	TF041-CAP;SPEAKER,HOUSING,A-7	
791941190152	TF041-LCD ASSY;COMMON,A790-7	
796119031006	TF041-BRKT HINGE;A-790	
796119060013	TF041-RUBBER PAD;HOOK,A-790	
796119062021	TF041-RUBBER PLUG;LCD,A-790	
796119092007	TF041-HOOK;A-790	
797425206000	TF041-WASH;M3,SPR,SUS,PSV	
796119060041	TF041-RUBBER FOOT;AS-136	
796119052026	TF041-WIRE MOUNT;FW-2S	
796121270051	TF041-DOW CORNING 3140 RTV SI	
796121270052	TF041-ADHESIVE SILICON RTV-31	
796119070027	TF041-SCR;M3L8,RND,SUS,PSV,6M	
791941190059	TF041-COVER ASSY;LCD,A790-73,	
796119070005	TF041-MAGNET;11.9*5.9*2MM,200	
796119091004	TF041-LCD COVER;12.1",GUNZE,A	
796119070009	TF041-TEMPERED GLASS;12.1,1AR	
796119071101	TF041-DOUBLE TAPE;3M,#4609,6M	
791931190001	TF041-KBD ASSY;A790,US,RUBBER	
796119062016	TF041-RUBBER KEY BD;BL,US,A79	
791911190070	TF041-PWA ASSY;A790,(A)KBD,W/	
411118200039	TF041-TH-PWA;PWA-A770,K/B,W/O	
411118200041	TF041-TH-PWA;PWA-A770,K/B,W/O	
272005105403	TF041-TH-CAP;0.1U,CR,50V,10%,	C500,C505

Part Number	Deacription	Location(S)
272043226507	TF041-TH-CAP;22U ,25V ,+-20%,	C501,C504
288104148020	TF041-TH-DIODE;RLS4148,200MA,	D500,D501
291000410409	TF041-TL-CON;HDR 4P,MA,SHROUD	J500
291000154019	TF041-TH-CON;FPC/FFC,40P,.7MM	J501
316118200010	TF041-PCB;PWA-A770,KBD MATRLI	R00
361200003204	TF041-SOLDER PASTE;PF606-P;FO	
242600000572	TF041-LABEL;4*3MM,HI-TEMP,260	
226683830006	TF041-CARTOON;L110,W290,H15,4	
365350000009	LF-SOLDER WIRE;SN96.5/AG3.0/C	
242600000566	TF041-LABEL;BLANK,7MM*7MM,PRC	
222672730004	TF041-PE BUBBLE BAG;230*370mm	
796119051001	TF041-MYLAR;KEYBOARD,A-790	
796119091002	TF041-BOTTOM COVER;KEYBOARD,A	
796119050001	TF041-TOP COVER;KEYBOARD,A-79	
791911190080	TF041-HOUSING ASSY;A790,(15)Y	
791941190130	TF041-HOUSING ASSY;COMMON,A79	
230000030047	TF041-RIBBON;13CM*300M,LABEL	
230000030048	TF041-RIBBON;11CM*300M,PT800	
242600000650	TF041-LABEL;25*10MM,POLYESTER	
242600000651	TF041-LABEL;25*10MM,3020F	
411119000010	TF041-TH- PWA;PWA-A790,PCMCIA	
411119000011	TF041-TH- PWA;PWA-A790,PCMCIA	
331040060012	TF041-TH-CON;HDR,MA,15P*4,1.2	J501
344600001135	TF041-IC CARD CON PART;68P*2,	
796119032003	TF041-BRACKET;BAY 1,CONNECT,A	

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Part Number	Deacription	Location(S)
796119042003	TF041-SPACER;MODEM,I/O,A-790	H7,H9
796115050082	TF041-SPACER;H=1,OUTER=3.7,IN	H501,H502
242600000567	TF041-LABEL;32*7MM,POLYESTER	
375102030012	TF041-NUT-HEX;M2,2,NIW	H20,H21
411119000012	TF041-TH- PWA;PWA-A790,PCMCIA	
272431157520	TF041-TH-CAP;150U,KOCAP,6.3V,	C143,C9
272105100307	TF041-TH-CAP;10P ,CR,50V ,5%	C11
272071225406	TF041-TH-CAP;2.2U ,CR,6.3V ,1	104,C118,C119,C144,C145C15,C9
272102104708	TF041-TH-CAP;0.1U ,16V,+80-2	10,C100,C108,C109,C114,12,C127
272101105705	TF041-TH-CAP;1U ,CR,6.3V ,8	106,C137,C138,C139,C209C26,C2
272001105410	TF041-TH-CAP;1U ,10%,10V ,0	C52,C58
272071334404	TF041-TH-CAP;0.33U ,10V ,10%,	C59,C62
272105220404	TF041-TH-CAP;22P ,50V ,+ -10	C63,C67,C70
272105101313	TF041-TH-CAP;100P ,50V ,5%,04	103,C110,C155,C156,C157C65,C6
272001106517	TF041-TH-CAP;10U,10V,+80-20%,	C130,C131,C150,C72,C96
272105102421	TF041-TH-CAP;1000P,CR,50V,10%	C165,C170,C171
272071475403	TF041-TH-CAP;4.7U,6.3V,10%,06	C107,C113
272101224702	TF041-TH-CAP;0.22U ,10V ,+80-	C121
272072474403	TF041-TH-CAP;0.47U,16V,10%,06	C122,C124,C125,C136
272072473409	TF041-TH-CAP;0.047U,16V ,10%,	C123
272431227006	TF041-TH-CAP;220uF,4V,7343,25	C151,C152
288105556002	TF041-TH-DIODE;BZV55-C5V6,ZEN	D12
295000010218	TF041-TH-FUSE;FAST,2A,63VDC,1	F5
291000611265	TF041-TH-MINI PCI SOCKET;124P	J5
291000410208	TF041-TL-CON;WFR,MA,2P,1.25,S	J6,J8

Part Number	Deacription	Location(S)
291000921202	TF041-TH-CON;MDC 12P,H=5MM,PI	J7
291000251504	TF041-TH-CON;IC CARD,75P*2,FM	J9
331840004006	TF041-TH-CON;STEREO JACK,4P,R	J10,J11
291000000905	TF041-TH-CON;MINI IEEE1394B,R	J12
291000011810	TF041-TH-CON;HDR,MA,90P*2,.8M	J502
288200144030	TF041-TH-TRANS;DDTC144TKA,N-M	Q5
271061000003	TF041-TH-RES;0 ,1/16W,0402	1,R10,R13,R17,R18,R19,R,R20,R2
271061472312	TF041-TH-RES;4.7K ,1/16W,5% ,	R11,R16,R4,R7
271061101109	TF041-TH-RES;100 ,1/16W,1% ,	R117,R21
271061272105	TF041-TH-RES;2.7K ,1/16W,1% ,	R86,R87
271061433306	TF041-TH-RES;43K ,1/16W,5% ,0	R34,R59
271061103307	TF041-TH-RES;10K ,1/16W,5% ,	100,R140,R41,R72,R94,R9
271061470502	TF041-TH-RES;47 ,1/16W,5% ,	R37,R39
271061473103	TF041-TH-RES;47K ,1/16W,1% ,	R136,R26,R44
271061203112	TF041-TH-RES;20K ,1/16W,1% ,	60,R61,R63,R64,R65,R66,80
271061102113	TF041-TH-RES;1K ,1/16W,1% ,	101,R105,R107,R110,R114R116,R
271061104306	TF041-TH-RES;100K ,1/16W,5% ,	133,R77,R81,R82,R91,R97
271061222104	TF041-TH-RES;2.2K,1/16W,1%,04	R84,R92,R93
271061334306	TF041-TH-RES;330K ,1/16W,5% ,	R89
271061221318	TF041-TH-RES;220 ,1/16W, 5%,	R119,R90
271061220308	TF041-TH-RES;22 ,1/16W,5% ,	R103,R14,R15,R99
271061632102	TF041-TH-RES;6.34K,1/16W,1% ,	R108
271061333304	TF041-TH-RES;33K ,1/16W,5% ,0	112,R113,R129,R130,R144
271061394307	TF041-TH-RES;390K ,1/16W,5% ,	R122
271061560106	TF041-TH-RES;56.2,1/16W,1%,04	R123,R124,R131,R132

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Part Number	Deacription	Location(S)
271061492102	TF041-TH-RES;4.99K,1/16W,1% ,	R134
271061105307	TF041-TH-RES;1M ,1/16W,5% ,	R145
284501520004	TF041-TH-IC;PCI1520,PCI/CARDB	U5
286302224001	TF041-TH-IC;TPS2224A,CARDBUS	U6
286104890003	TF041-TH-IC;AUDIO AMPLIFIER,L	U9
284501394003	TF041-TH-IC;1394B CONTROLLER	U10
284500260006	TF041-TH-IC;ALC260,AUDIO CODE	U11
286303301003	TF041-TH- IC;ADP3301AR-5 SO8	U12
284501394004	TF041-TH-IC;1394B PHY,TSB81BA	U13
286100212002	TF041-TH-IC;TPA0212,AMPLIFIER	U14
274040304401	TF041-TH-OSC;98.304MHZ,3.3V,7	X5
316119000004	TF041-TH- PCB;PWA-A790,PCMCIA	R01
242600000572	TF041-LABEL;4*3MM,HI-TEMP,260	
242600000654	TF041-LABEL;27*7MM,HI-TEMP 26	
271061131109	TF041-TH-RES;130 ,1/16W,1% ,	R115
272011226706	TF041-TH-CAP;22U ,CR,10V,1206	C115,C25,C34,C8
273000150374	TF041-TH-FERRITE CHIP;120OHM/	10,L11,L12,L13,L15,L18,19,L20,L
288101005003	TF041-TH-DIODE ; ESD. V-PORT-	15,D16,D17,D19,D20,D6,D,D8,D9
283468470001	TF041-TH-IC;EEPROM,M24C02-WMN	U8
291000152621	TF041-THCON;FPC/FFC,26P,.5MM,	J20
272021226707	TF041-TH-CAP;22U ,10V,+80-20	C1
271061822307	TF041-TH-RES;8.2K ,1/16W,5% ,	R194,R196
272105271406	TF041-TH-CAP;270P ,50V,+/-10%,	C141,C142
282574132012	TF041-TH-IC;74AHCT1G32,SINGLE	U1,U2
271061196215	TF041-TH-RES;19.6K,1/16W,1%,0	R141

Part Number	Deacription	Location(S)
288179301001	TF041-TH-IC;TPS79301DBVR ,TL	U17
288103050001	TF041-TH-ESD DIODE; PD03S050	D18,D21,D22,D23
271061204104	TF041-TH-RES;200K ,1/16W,1% ,	R69
288100056028	TF041-TH-DIODE;RLZ5.6B,ZENER,	D5
272101016401	TF041-TH-CAP;.1U ,CR,10V,10%	C200,C201,C204,C210
796119012011	TF041-S-STANDOFF;H=5MM,A-SER	H20,H21
796119040012	TF041-SPRING;PCMCIA CON,A790	
281307125007	TF041-TH-IC;NC7SZ125,SINGLE,S	
411119000013	TF041-TH-PWA;PWA-A790 BATT3 T	
411119000014	TF041-TH-PWA;PWA-A790 BATT3 T	
411119000015	TF041-TH-PWA;PWA-A790 BATT3 T	
316119000005	TF041-TH-PCB;PWA-A790 BATT3 T	R01
331000007083	TF041-CON;BATTERY,7P,MA,2.5MM	PJ201
242600000572	TF041-LABEL;4*3MM,HI-TEMP,260	
291000410803	TF041-TL-CON;WFR,MA,8P*1,1.25	PJ200
411119000019	TF041-TH-PWA;PWA-A790 BATTERY	
411119000020	TF041-TH-PWA;PWA-A790 BATTERY	
411119000021	TF041-TH-PWA;PWA-A790 BATTERY	
272072474403	TF041-TH-CAP;0.47U,16V,10%,06	PC1,PC18,PC2
272075104710	TF041-TH-CAP;0.1U ,50V,+80-2	C14,PC17,PC22,PC26,PC27PC28,
272013106504	TF041-TH-CAP;10U,25V,+/-20%,1	PC12,PC16,PC5
272043226507	TF041-TH-CAP;22U ,25V ,+/-20%,	PC15,PC7
272001106517	TF041-TH-CAP;10U,10V,+80-20%,	PC11,PC20,PC9
272003105402	TF041-TH-CAP;1U ,CR,25V ,10	PC10,PC21,PC25
272101104415	TF041-TH-CAP;0.1U ,CR,10V,10	PC13

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Part Number	Deacription	Location(S)
272002225401	TF041-TH-CAP;2.2U ,16V ,10%,0	PC24,PC501
288100099015	TF041-TH-DIODE;BAV99,70V,450M	D1,PD19,PD2,PD20,PD5,PD
288100054034	TF041-TH-DIODE;BAT54,30V,200m	PD11,PD7
288100034012	TF041-TH-DIODE;SSA34,40V,3A,S	D10,PD22,PD23,PD25,PD50,PD50
288100701003	TF041-TH-DIODE;BAV70LT1,70V,2	PD507,PD508
295000010243	TF041-TH-FUSE;NANO,10A/125V,R	PF1
273000990374	TF041-TH-INDUCTOR;4.7UH,D104C	PL500,PL501
288206679005	TF041-TH-TRANS;FDS6679_NL,P-M	Q1,PQ16,PQ2,PQ500,PQ501PQ50
288204832002	TF041-TH-TRANS;SI4832DY,N-MOS	PQ5
288227002024	TF041-TH-TRANS;2N7002LT1,N-CH	PQ10,PQ13,PQ14,PQ15,PQ7
288204835008	TF041-TH-TRANS;SI4835BDY-T1-E	PQ11,PQ12
271072118311	TF041-TH-RES;118K ,1/10W,1% ,	PR2
271046257104	TF041-TH-RES;025 ,2W ,1% ,25	PR29,PR3
271061000003	TF041-TH-RES;0 ,1/16W,0402	R30,PR31,PR44,PR48,PR5,R7
271061303103	TF041-TH-RES;30K ,1/16W,1% ,0	PR6,PR8
271061103114	TF041-TH-RES;10K ,1/16W,1% ,	R13,PR15,PR18,PR21,PR42PR9
271072100310	TF041-TH-RES;10 ,1/10W,5% ,	R12,PR14,PR17,PR43,PR49PR500
271061373102	TF041-TH-RES;37.4K,1/16W,1% ,	PR16
271061114102	TF041-TH-RES;113K ,1/16W,1% ,	PR19,PR20,PR35
271061102113	TF041-TH-RES;1K ,1/16W,1% ,	PR22,PR38
271061184304	TF041-TH-RES;180K ,1/16W, 5%	PR23
271061204104	TF041-TH-RES;200K ,1/16W,1% ,	R24,PR37,PR40,PR50,PR51
271045029102	TF041-TH-RES;02 ,1W,1%,2512,	PR25,PR46
271061123106	TF041-TH-RES;12.1K ,1/16W,1%	PR26,PR41
271061474304	TF041-TH-RES;470K ,1/16W,5% ,	R27,PR34,PR36,PR39,PR40PR45,

Part Number	Deacription	Location(S)
271061223105	TF041-TH-RES;22K,1/16W,1% ,04	PR28,PR47
271061105307	TF041-TH-RES;1M ,1/16W,5% ,	PR32
271071344103	TF041-TH-RES;340K ,1/16W,1% ,	PR33
282574405205	TF041-TH-IC;74HC4052MX_NL,DUA	PU1
286000864002	TF041-TH-IC;OZ864,DUAL BATT C	PU2
286000860001	TF041-TH-IC;OZ860,SINGLE BATT	PU3
316119000007	TF041-TH-PCB;PWA-A790 BATTERY	R01
242600000572	TF041-LABEL;4*3MM,HI-TEMP,260	
271071494101	TF041-TH-RES;499K ,1/16W,1% ,	PR1
331040007008	TF041-TH-CON;BATTERY,7P,MA,2.	PJ502
288202303008	TF041-TH-TNANS;SI2303,P-MOSFE	PQ17
291000410803	TF041-TL-CON;WFR,MA,8P*1,1.25	PJ505
331030008058	TF041-TH-CON;HDR,MA,4P*2,2.54	PJ501,PJ503
331030020043	TF041-TH-CON;HDR,MA,10P*2,2.5	PJ504
422118200024	TF041-TH-CABLE ASSY;SPEAKER R	
422118200025	TF041-TH-CABLE ASSY;SPEAKER L	
796118260001	TF041-EMI GASKET;LAN CONNECTO	
796119002001	TF041-HDD CAP ASSY;A770	
796119002002	TF041-BATTERY CAP ASSY;A-790	
796119002003	TF041-BRACKET;I/O ASSY,A-790	
796119002004	TF041-HEATSINK-MODULE-1,A790	
796119010001	TF041-DOOR HINGE;SUS,A-790	
796119010002	TF041-SHOULDER SCREW;A-790	
796119010010	TF041-SCREW;EJECTOR,M2,A-790	
796119012002	TF041-HOLDER;2ND SCREW,A-790	

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Part Number	Deacription	Location(S)
272002225401	TF041-TH-CAP;2.2U ,16V ,10%,0	PC24,PC501
288100099015	TF041-TH-DIODE;BAV99,70V,450M	D1,PD19,PD2,PD20,PD5,PD
288100054034	TF041-TH-DIODE;BAT54,30V,200m	PD11,PD7
288100034012	TF041-TH-DIODE;SSA34,40V,3A,S	D10,PD22,PD23,PD25,PD50,PD50
288100701003	TF041-TH-DIODE;BAV70LT1,70V,2	PD507,PD508
295000010243	TF041-TH-FUSE;NANO,10A/125V,R	PF1
273000990374	TF041-TH-INDUCTOR;4.7UH,D104C	PL500,PL501
288206679005	TF041-TH-TRANS;FDS6679_NL,P-M	Q1,PQ16,PQ2,PQ500,PQ501PQ50
288204832002	TF041-TH-TRANS;SI4832DY,N-MOS	PQ5
288227002024	TF041-TH-TRANS;2N7002LT1,N-CH	PQ10,PQ13,PQ14,PQ15,PQ7
288204835008	TF041-TH-TRANS;SI4835BDY-T1-E	PQ11,PQ12
271072118311	TF041-TH-RES;118K ,1/10W,1% ,	PR2
271046257104	TF041-TH-RES;025 ,2W ,1% ,25	PR29,PR3
271061000003	TF041-TH-RES;0 ,1/16W,0402	R30,PR31,PR44,PR48,PR5,R7
271061303103	TF041-TH-RES;30K ,1/16W,1% ,0	PR6,PR8
271061103114	TF041-TH-RES;10K ,1/16W,1% ,	R13,PR15,PR18,PR21,PR42PR9
271072100310	TF041-TH-RES;10 ,1/10W,5% ,	R12,PR14,PR17,PR43,PR49PR500
271061373102	TF041-TH-RES;37.4K,1/16W,1% ,	PR16
271061114102	TF041-TH-RES;113K ,1/16W,1% ,	PR19,PR20,PR35
271061102113	TF041-TH-RES;1K ,1/16W,1% ,	PR22,PR38
271061184304	TF041-TH-RES;180K ,1/16W, 5%	PR23
271061204104	TF041-TH-RES;200K ,1/16W,1% ,	R24,PR37,PR40,PR50,PR51
271045029102	TF041-TH-RES;02 ,1W,1%,2512,	PR25,PR46
271061123106	TF041-TH-RES;12.1K ,1/16W,1%	PR26,PR41
271061474304	TF041-TH-RES;470K ,1/16W,5% ,	R27,PR34,PR36,PR39,PR40PR45,

Part Number	Deacription	Location(S)
796119012006	TF041-S-STANDOFF;H=18MM,A-790	
796119012007	TF041-DOOR BRACKET;I/O,A-790	
796119019001	TF041-SPRING FINGER;BAY1,HOUS	
796119030035	TF041-DEPRESS;LOCKER,A-790	
796119031003	TF041-DOOR;BAY1,SUS PIN,A-790	
796119032001	TF041-DOOR;I/O,A-790	
796119050002	TF041-CAP;IR,A-790	
796119050011	TF041-MYLAR;BATTERY-HOUSING,A	
796119050050	TF041-EJECTER;A-790	
796119051015	TF041-MYLAR;EJECTOR,A-790	
796119052001	TF041-DOOR LOCK (TIFCO F091Y)	
796119052009	TF041-CAP;PCMCIA,PARTITION-YO	
796119052004	TF041-CAP;CHARGER,PARTITION,A	
796119052010	TF041-MYLAR;SPEAKER,14.1",A-7	
796119052011	TF041-MYLAR;BATTERY,A-790	
796119052023	TF041-MYLAR;HOUSING 5.0x4.0x0	
796119060001	TF041-RUBBER;SPEAKER,A-790	
796119060002	TF041-RUBBER PAD;BAY1,A-790	
796119060003	TF041-RUBBER PAD;BAY1 DOOR,A-	
796119060009	TF041-RUBBER;FDD,A-790	
796119060015	TF041-HANDLE;A-790	
796119060017	TF041-RUBBER PAD;HEAT SINK,A-	
796119060031	TF041-RUBBER;25*25*0.5T,A-790	
796119060032	TF041-RUBBER;9卅*3t(蚬蠟AR-34	
796119060205	TF041-RUBBER;BAY 1,IP54,A-790	

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Part Number	Deacription	Location(S)
796119061020	TF041-RUBBER;DOOR LOCK,8*3.5*	
796119062032	TF041-SPONG;34*8*2T,A-790	
796119062041	TF041-DOOR;RUBBER,POWER,A-790	
796119062042	TF041-DOOR;RUBBER,USB,A-790	
796119062043	TF041-DOOR;RUBBER,VGA,A-790	
796119062044	TF041-DOOR;RUBBER,LAN,A-790	
796119062045	TF041-DOOR;RUBBER,SIO,A-790	
796119062046	TF041-DOOR;RUBBER,PIO,A-790	
796119062047	TF041-DOOR;RUBBER,PORT REPLIC	
796119062048	TF041-RUBBER;I/O DOOR,A-790	
796119062049	TF041-CAP;DD,PARTITION,A-790	
796119062051	TF041-SPONGE;PCMCIA CAP,A-790	
796119062053	TF041-SPONGE;3*295*3,A-790	
796119067001	TF041-RUBBER PAD;70*9*2t,BAY1	
796119070006	TF041-TAPE;25MM*45M, CM34	
796119070010	TF041-LABEL;104*69MM,PANTONE	
796119070014	TF041-DUO-PAK,DP-420,OFF-WHIT	
796119090002	TF041-HOUSING-YONAH;A790	
796119092010	TF041-BRKT;RH,HOLDER,A-790	
796119092011	TF041-BRKT;LF,HOLDER,A-790	
797746444045	TF041-S-STANDOFF;#4-40 ψ4L4*	
796119061048	TF041-RUBBER;MB-HEATSINK,A790	
796119061049	TF041-RUBBER;IO BD-COVER CHAS	
412806000002	TF041-FAX MODEM 56K,RD02-D330	
796119064010	TF041-COND TAPE; 85773, DDR C	

Part Number	Deacription	Location(S)
796119064009	TF041-GASKET; 773GT, DDR CONT	
796119071004	TF041-GASKET;ψ1.8,A790	
422119000014	TF041-CABLE ASSY;BAT3 TRANS C	
422119000015	TF041-TH-CABLE ASSY A790 MODE	
796119051016	TF041-MYLAR;150*22*0.1,A-SER	
796119061055	TF041-Rubber;10*10*9.2,A790	
411119000070	TF041-TH-PWA;PWA-A790,ST DD B	
411119000071	TF041-TH-PWA;PWA-A790,ST DD B	
411119000072	TF041-TH-PWA;PWA-A790,ST DD B	
272043226507	TF041-TH-CAP;22U ,25V ,+-20%,	C8
272075104710	TF041-TH-CAP;0.1U ,50V,+-80-2	C9
272071225406	TF041-TH-CAP;2.2U ,CR,6.3V ,1	C502
272071105412	TF041-TH-CAP;1U,10V,10%,0603,	C10,C501
288105232007	TF041-TH-DIODE;MMSZ5232B,5.6V	D2
291000015406	TF041-TL-CON;HDR,FM,P=1.0,H=2	J501
273000500187	TF041-TH-FERRITE CHIP;120OHM/	L16,L17
288202301008	TF041-TH-TRANS;SI2301BDS,P-MO	Q5
288100099015	TF041-TH-DIODE;BAV99,70V,450M	D7,D8
288200144029	TF041-TH-TRANS;DTC144WK,NPN,S	Q503
286300809025	TF041-TH IC;ADM809SART-REEL7	U505
288227002024	TF041-TH-TRANS;2N7002LT1,N-CH	Q10,Q502
286300055003	TF041-TH-IC;TC555,3.3V,250mA,R	U504
271072118311	TF041-TH-RES;118K ,1/10W,1% ,	R3
271061104108	TF041-TH-RES;100K ,1/16W,1% ,	R501,R515,R6,R8
271061474304	TF041-TH-RES;470K ,1/16W,5% ,	R7

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Part Number	Deacription	Location(S)
271061105104	TF041-TH-RES;1M,1/16W,1% ,040	R502,R9
286302951002	TF041-TH-IC;LP2951CM_NL,VOLTA	U5
288206679005	TF041-TH-TRANS;FDS6679_NL,P-M	U6
316119000008	TF041-TH-PCB;PWA-A790 ST DD W	R01
242600000572	TF041-LABEL;4*3MM,HI-TEMP,260	
331040007008	TF041-TH-CON;BATTERY,7P,MA,2.	J3
271071494101	TF041-TH-RES;499K ,1/16W,1% ,	R4
288100701003	TF041-TH-DIODE;BAV70LT1,70V,2	D6
331030008057	TF041-TH-CON;HDR,FM,4P*2,2.54	J1,J2
331030020042	TF041-TH-CON;HDR,FM,10P*2,2.5	J4
796119052014	TF041-PARTITION+ES;BAY 1,A-79	
796119060020	TF041-RUBBER CUSHION;A-790	
796119060019	TF041-RUBBER PAD 13.2*14.7*1;	
797626435118	TF041-S-STANDOFF;M3L11*8,NIW	
796118270008	TF041-THERMAL PAD; SB, Catero	
796119061062	TF041-RUBBER;10*7*4,A790	
796118270005	TF041-THERMAL PAD; ICS, A770;	
796119070043	TF041-MYLAR;30*80*0.5T,A790	
791941182200	TF041-FDD ASSY;A-770,1.44MB,B	
791941182201	TF041-CANISTER;FDD,A770	
411118200046	TF041-TH-PWA;PWA-A770 BAY1 FD	
316118200014	TF041-TH- PCB;PWA-A770 BAY1 F	R00
331040060013	TF041-TH-CON;HDR,15P*4,FM,1.2	J1
797215202016	TF041-NUT;M2,HEX,SUS,PSV	
242600000572	TF041-LABEL;4*3MM,HI-TEMP,260	

Part Number	Deacription	Location(S)
226683830006	TF041-CARTOON;L110,W290,H15,4	
222672730002	TF041-PE BUBBLE BAG;BATTERY,2	
796119011007	TF041-COVER;EXTERNAL FDD,BK,A	
796119090013	TF041-HOLDER;BAY1,A-790	
242600000651	TF041-LABEL;25*10MM,3020F	
796119030070	TF041-BRKT;FDD,BAY1,A-790	
796119069002	TF041-RUBBER PAD;30*5*1.5T,A-	
523430075014	TF041-TH-FDD ASSY;1MB,1.6MB O	
411119000041	TF041-TH-PWA;PWA-A790 M/B	
411119000042	TF041-TH-PWA;PWA-A790 M/B,T/U	
411119000043	TF041-TH-PWA;PWA-A790 M/B,SMT	
272013106504	TF041-TH-CAP;10U,25V,+/-20%,1	C11,C2
272105102421	TF041-TH-CAP;1000P,CR,50V,10%	C4,C8
272101104415	TF041-TH-CAP;0.1U ,CR,10V,10	10,C114,C115,C118,C123,125,C12
272071225406	TF041-TH-CAP;2.2U ,CR,6.3V ,1	126,C13,C132,C133,C147,148,C15
272102104708	TF041-TH-CAP;0.1U ,16V,+80-2	14,C16,C329,C330,C331,C83,C38
272401107507	TF041-TL-CAP;100U,POSCAP,4V,2	131,C17,C214,C26,C264,C4
272101473407	TF041-TH-CAP;0.047U,10V,10%,0	30,C32,C533,C534,C535,C36,C53
272001106404	TF041-TH-CAP;10U,6.3V ,10%,08	12,C120,C121,C130,C178,188,C18
272102223409	TF041-TH-CAP;0.022U,16V ,+-10	117,C36,C38,C40,C519,C58,C530
272103103407	TF041-TH-CAP;0.01U ,CR,25V ,1	175,C42,C44,C45,C47,C50,C512,C
272101015402	TF041-TH-CAP;1U,6.3V,+/-10%,04	138,C142,C143,C197,C198C275,C
272071475403	TF041-TH-CAP;4.7U,6.3V,10%,06	128,C194,C31,C328,C33,C0,C501
272101224702	TF041-TH-CAP;0.22U ,10V ,+80-	C119,C55
272101474703	TF041-TH-CAP; 0.47U ,CR,10V,+	C122,C124

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Part Number	Deacription	Location(S)
272105180308	TF041-TH-CAP;18P ,50V ,+/-5%	C377,C378
272431227545	TF041-TH-CAP;220U,2.5V,TPE-MC	429,C500,PC510,PC527,PC38,PC5
272105392502	TF041-TH-CAP;3900P,50V,+/-20%	307,C308,C309,C310,C588C589,C
272002105709	TF041-TH-CAP;1U ,CR,16V ,-20	C379,C380
272431157520	TF041-TH-CAP;150U,KOCAP,6.3V,	127,C172,C176,C221,C274C603
272105222411	TF041-TH-CAP;2200P,50V ,+/-10	C513,C514
272105220404	TF041-TH-CAP;22P ,50V ,+ -10	C598,C599
288100054034	TF041-TH-DIODE;BAT54,30V,200m	1,D10,D13,D2,D4,D5,D507D508,I
288100541004	TF041-TH-DIODE;BAT54ALT1,COM.	D3,D506
288100099015	TF041-TH-DIODE;BAV99,70V,450M	D14,D7,D8
288100054035	TF041-TH-DIODE;BAT54C,SCHOTTK	D12
291000010049	TF041-TL-CON;HDR,FM,40P,0.5MM	J1
291000015206	TF041-TL-CON;HDR,MA,P=1.0,H=2	J6
291000011236	TF041-TL-CON;HDR,MA P=0.5 H=4	J4,J5,J7
291000015405	TF041-TL-CON;HDR,MA,P=1.0,H=2	J8
291000015603	TF041-TL-CON;HDR,FM P=0.8 H=5	J501,J505
291000612036	TF041-TL-CON;DDR2 STD SOCKET	J504
291000612034	TF041-TL-CON;DDR2 STD SOCKET	J503
291000020233	TF041-TL-CON;HDR,MA,2P*1,1.25	J506
273000130360	TF041-TH-FERRITE CHIP;120OHM/	15,L16,L22,L4,L501,L505L510
272073104712	TF041-TH-CAP;0.1U,25V,10%,060	C23,C116,PC27,PC34,PC35PC36,I
272075102419	TF041-TH-CAP;1000P,CR,50V,10%	C15,PC19,PC31,PC32,PC48PC51,I
272431477003	TF041-TH-CAP;470U,2.5V,2R5TPE	427,C430,PC10,PC505,PC56,PC50
272075100404	TF041-TH-CAP;10P ,50V ,10%,0	PC11
272075103414	TF041-TH-CAP;0.01U ,CR,50V ,1	PC14,PC16,PC20,PC25

Part Number	Deacription	Location(S)
272075101408	TF041-TH-CAP;100P ,50V ,10%,0	PC24,PC30
272075152405	TF041-TH-CAP;1500P,CR,50V,10%	PC26
272431336001	TF041-TH-CAP;330uF,6.3V,7343,	C511,PC512,PC520,PC543,C544
272431157518	TF041-TH-CAP;150U ,TPC,6.3V,2	PC519
272075221411	TF041-TH-CAP;220P ,CR,50V ,10	PC542
288100034012	TF041-TH-DIODE;SSA34,40V,3A,S	D1,PD11,PD5,PD501,PD504PD6
288100540006	TF041-TH-DIODE;MBR0540 _NL,1A,	D2,PD3,PD4,PD502,PD503,D7,PD
295000010206	TF041-TH-FUSE;NORMAL,6.5A/32V	PF1
273000990377	TF041-TH-INDUCTOR;0.82UH,FDU1	PL501,PL502
273000990374	TF041-TH-INDUCTOR;4.7UH,D104C	L503,PL504,PL505,PL509,L511
288207821006	TF041-TH-TRANS;IRF7821PBF,N-M	Q1,PQ10,PQ11,PQ3,PQ5,PQ03,PQ
288207832004	TF041-TH-TRANS;IRF7832PBF,N-M	Q2,PQ20,PQ4,PQ502,PQ505PQ50
288203415002	TF041-TH-TRANS;AO3415,P-MOSFE	PQ16,PQ17,PU501
288227002024	TF041-TH-TRANS;2N7002LT1,N-CH	Q18,PQ19,PQ507,Q1,Q3,Q5Q501,
271061000003	TF041-TH-RES;0 ,1/16W,0402	PR14,R8,PR16,PR17,PR18,PR19,F
271002752103	TF041-TH-RES;RES;7.5K ,1/8W,	PR34,PR9
271061104108	TF041-TH-RES;100K ,1/16W,1% ,	R10,PR21,PR30,PR504,PR5,PR53
271061100103	TF041-TH-RES;10,1/16W,1%,0402	R11,PR12,PR13,PR26,PR27PR49,
271061105104	TF041-TH-RES;1M,1/16W,1% ,040	R28,PR32,PR50,PR524,PR56,PR5
271071150104	TF041-TH-RES;15 ,1/16W,1% ,06	PR29
271061102113	TF041-TH-RES;1K ,1/16W,1% ,	R31,PR502,PR53,R213,R23R296,I
271072562104	TF041-TH-RES;5.6K ,1/10W,1% ,	PR43
271013221302	TF041-TH-RES;220 ,1/4W,5% ,1	PR503,PR54
271046017302	TF041-TH-RES;.001,2W,5%,2512,	PR507,PR508
271061474304	TF041-TH-RES;470K ,1/16W,5% ,	R45,PR48,PR51,PR60,R10

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Part Number	Deacription	Location(S)
272105180308	TF041-TH-CAP;18P ,50V ,+/-5%	C377,C378
272431227545	TF041-TH-CAP;220U,2.5V,TPE-MC	429,C500,PC510,PC527,PC38,PC5
272105392502	TF041-TH-CAP;3900P,50V,+/-20%	307,C308,C309,C310,C588C589,C
272002105709	TF041-TH-CAP;1U ,CR,16V ,-20	C379,C380
272431157520	TF041-TH-CAP;150U,KOCAP,6.3V,	127,C172,C176,C221,C274C603
272105222411	TF041-TH-CAP;2200P,50V ,+/-10	C513,C514
272105220404	TF041-TH-CAP;22P ,50V ,+ -10	C598,C599
288100054034	TF041-TH-DIODE;BAT54,30V,200m	1,D10,D13,D2,D4,D5,D507D508,I
288100541004	TF041-TH-DIODE;BAT54ALT1,COM.	D3,D506
288100099015	TF041-TH-DIODE;BAV99,70V,450M	D14,D7,D8
288100054035	TF041-TH-DIODE;BAT54C,SCHOTTK	D12
291000010049	TF041-TL-CON;HDR,FM,40P,0.5MM	J1
291000015206	TF041-TL-CON;HDR,MA,P=1.0,H=2	J6
291000011236	TF041-TH-CON;HDR,MA P=0.5 H=4	J4,J5,J7
291000015405	TF041-TL-CON;HDR,MA,P=1.0,H=2	J8
291000015603	TF041-TH-CON;HDR,FM P=0.8 H=5	J501,J505
291000612036	TF041-TH-CON;DDR2 STD SOCKET	J504
291000612034	TF041-TH-DIMM SOCKET;DDRII RE	J503
291000020233	TF041-TL-CON;HDR,MA,2P*1,1.25	J506
273000130360	TF041-TH-FERRITE CHIP;120OHM/	15,L16,L22,L4,L501,L505L510
272073104712	TF041-TH-CAP;0.1U,25V,10%,060	C23,C116,PC27,PC34,PC35PC36,I
272075102419	TF041-TH-CAP;1000P,CR,50V,10%	C15,PC19,PC31,PC32,PC48PC51,I
272431477003	TF041-TH-CAP;470U,2.5V,2R5TPE	427,C430,PC10,PC505,PC56,PC50
272075100404	TF041-TH-CAP;10P ,50V ,10%,0	PC11
272075103414	TF041-TH-CAP;0.01U ,CR,50V ,1	PC14,PC16,PC20,PC25

Part Number	Deacription	Location(S)
271071153105	TF041-TH-RES;15K ,1/16W,1% ,	PR66
271071101107	TF041-TH-RES;100 ,1/16W,1% ,	PR505,PR506
271071362102	TF041-TH-RES;3.6K ,1/16W,1% ,	PR511,PR525
271072113312	TF041-TH-RES;113K ,1/10W,1% ,	PR512
271071712102	TF041-TH-RES;7.15K ,1/16W,1%	PR515
271061402214	TF041-TH-RES;40.2K,1/16W,1% ,	PR516
271071133104	TF041-TH-RES;13.3K,1/16W,.1%,	PR520
271071513102	TF041-TH-RES;51K ,1/16W,1% ,	PR521
271071184103	TF041-TH-RES;180K ,1/16W,1% ,	PR523
271061223105	TF041-TH-RES;22K,1/16W,1% ,04	PR530
271071604115	TF041-TH-RES;6.04K,1/16W,1% ,	PR532
271072118311	TF041-TH-RES;118K ,1/10W,1% ,	PR534
271061203112	TF041-TH-RES;20K ,1/16W,1% ,	R514,PR517,PR522,PR529,239
286300452001	TF041-TH-IC;SC452,PWM CONTROL	PU1
286300480001	TF041-TH-IC;SC480,PWM-DDR2,ML	PU2
286104173002	TF041-TH-IC;MAX4173F,I-SENSE	PU4
286301485001	TF041-TH-IC;SC1485,PWM,TSSOP-	PU502,PU504
286302731001	TF041-TH-IC;LM2731YMF,Boost C	PU503
288200144029	TF041-TH-TRANS;DTC144WK,NPN,S	PQ501,Q2,Q7
288200144030	TF041-TH-TRANS;DDTC144TKA,N-M	11,Q12,Q502,Q503,Q505,Q
271621103306	TF041-TH-RP;10K*8 ,10P,1/32W,	RP1
271621472306	TF041-TH-RP;4.7K*8,10P,1/32W,	RP2
271061228102	TF041-TH-RES;2.2,1/16W,1%,040	R3
271061471308	TF041-TH-RES;470 ,1/16W,5% ,	R4
271061473103	TF041-TH-RES;47K ,1/16W,1% ,	R7,R8,R9

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Part Number	Deacription	Location(S)
271061103114	TF041-TH-RES;10K ,1/16W,1% ,	R1,PR2,PR22,PR4,PR5,R11R12,R
271061222104	TF041-TH-RES;2.2K,1/16W,1%,04	190,R193,R25,R42,R522,R55,R87
271061330311	TF041-TH-RES;33 ,1/16W,5% ,	127,R128,R129,R130,R131R134,R
271071228306	TF041-TH-RES;2.2 ,1/16W,5% ,	R34,R74
271061750105	TF041-TH-RES;75,1/16W,1%,0402	R40
271071100103	TF041-TH-RES;10 ,1/16W,1% ,	R41,R85
271061201107	TF041-TH-RES;200 ,1/16W, 1% ,	R49
271061800101	TF041-TH-RES;80.6,1/16W,1%,04	R51,R52
271061560306	TF041-TH-RES;56 ,1/16W,5% ,	100,R101,R102,R103,R104R105,R
271061220308	TF041-TH-RES;22 ,1/16W,5% ,	R521,R554,R76
271061540102	TF041-TH-RES;54.9 ,1/16W,1% ,	157,R158,R159,R160,R173R174,R
271061240102	TF041-TH-RES;24.9,1/16W,1% ,0	163,R187,R508,R519,R589R623
271061472312	TF041-TH-RES;4.7K ,1/16W,5% ,	171,R203,R258,R262,R263R265,R
271061270104	TF041-TH-RES;27.4 ,1/16W, 1% ,	R175,R513
271061822307	TF041-TH-RES;8.2K ,1/16W,5% ,	180,R188,R206,R207,R208R209,R
271061202104	TF041-TH-RES;2K ,1/16W,1% ,	R510
271061334103	TF041-TH-RES;332K,1/16W,1%,04	R243
271061390309	TF041-TH-RES;39, 1/16W, 5%,0	170,R176,R195,R246,R247R250,R
271061106308	TF041-TH-RES;10M ,1/16W,5% ,	R289
271061510306	TF041-TH-RES;51, 1/16W, 5%,0	R514
271071000312	TF041-TH-RES;0 ,1/16W,5% ,	R517
271061492102	TF041-TH-RES;4.99K,1/16W,1% ,	R531
271061010102	TF041-TH-RES;1,1/16W,1%,0402,	R535,R577
271061152502	TF041-TH-RES;1.5K ,1/16W,5% ,	R567
271061101109	TF041-TH-RES;100 ,1/16W,1% ,	R36,PR7,R155,R156,R17,R78,R18

Part Number	Deacription	Location(S)
271071220308	TF041-TH-RES;22 ,1/16W,5% ,	R681
288003602002	TF041-TH-FIR; HSDL-3602-007 F	U1
284509310001	TF041-TH-IC;ICS9LPR310, LOW P	U2
281307085005	TF041-TH-IC;NC7SZ08P5,2-INPUT	U3,U4
286369229003	TF041-TH-IC;G692L293Tf,RESET	U5
286301117092	TF041-TH-IC;AME1117BCGTZ,2.5V	U501
282000302001	TF041-TH-IC;LIS3L02DQ,G-SENSO	U502
284500007017	TF041-TH-IC;ICH7M,SOUTH BRIDG	U506
291000613223	TF041-TH-IC SOCKET;32P,PLCC,T	U508
481119000002	TF041-F/W ASSY;KBD CTRL,H8,A7	U509
284564214002	TF041-TH-IC;H8S/2140B,KBD CTR	
242600000648	TF041-LABEL;10*8MM,BIOS,HI-TE	
274011431467	TF041-TH-XTAL;14.318MHZ,16PF,	X1
274013275401	TF041-TH-XTAL;32.768KHZ,20PPM	X3
274011000412	TF041-TH-XTAL;10M,30PPM,16PF,	X501
316119000002	TF041-TH-PCB;PWA-A790,M/B	R01
271046257104	TF041-TH-RES;.025 ,2W ,1% ,25	PR63
271061221107	TF041-TH-RES;221,1/16W,1%,040	R16,R506
272105120310	TF041-TH-CAP;12P ,CR,50V ,5%	C28,C29
272071105412	TF041-TH-CAP;1U,10V,10%,0603,	387,C597,PC12,PC17,PC18PC28,F
273000990296	TF041-TH-INDUCTOR;10UH,+,-20%,	L11,L504
272011226706	TF041-TH-CAP;22U ,CR,10V,1206	C171,C539
242600000572	TF041-LABEL;4*3MM,HI-TEMP,260	
242600000654	TF041-LABEL;27*7MM,HI-TEMP 26	
242600000676	TF041-LABEL;25*6MM,COMMON	

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Part Number	Deacription	Location(S)
273000150374	TF041-TH-FERRITE CHIP;120OHM/	1,L10,L12,L2,L27,L3,L31L5,L502,
271061251102	TF041-TH-RES;255,1/16W,1%,040	R81
273000990375	TF041-TH-INDUCTOR;4.7UH,FDV06	PL508
272075620302	TF041-TH-CAP;62P ,CR,50V ,5%	PC13
271072303102	TF041-TH-RES;30K ,1/10W,1% ,0	PR3
284180786068	TF041-TH-IC;CPU,YONAH,LV,1.66	U504
286301022001	TF041-TH IC;ADM1022ARQ QSOP-1	U503
288202303008	TF041-TH-TNANS;SI2303,P-MOSFE	PQ506
272433156506	TF041-TH-CAP;15U,25V,20%,60M,	C100,PC102,PC103,PC49,P525,PC
291000011227	TF041-TL-CON;WFR,MA,12P,1.25M	J502
271061681308	TF041-TH-RES;680 ,1/16W,5% ,	PR555
272105101313	TF041-TH-CAP;100P ,50V ,5%,04	PC84,PC85
272105472406	TF041-TH-CAP;4700PF,50V,10%,0	C604
271061223106	TF041-TH-RES;22.1K,1/16W,1% ,	PR20
271071134102	TF041-TH-RES;130K ,1/16W,1% ,	PR15
272431227576	TF041-TH-CAP;220uF,2.5V,+,-20%	103,C160,C192,C223,C224C225
288100056028	TF041-TH-DIODE;RLZ5.6B,ZENER,	PD15
271061220105	TF041-TH-RES;22 ,1/16W,1% ,	136,R138,R139,R141,R143R146,R
796119041001	TF041-SPACER;VGA BD,A-790	H3,H5,H6
272000226501	TF041-TH-CAP;22U ,CR,6.3V,080	100,C101,C102,C104,C105C106,C
284500945002	TF041-TH-IC;945GM,NORTH BRIDG	U505
481119000001	TF041-F/W ASSY;SYS/VGA BIOS,A	
283460000018	TF041-TH-IC;FLASH,IM*8,FWH,SS	
421118200001	TF041-WIRE ASSY;BIOS,BATTERY	
411119000100	TF041-TH-PWA;PWA-A790 M/B CLO	

Part Number	Deacription	Location(S)
411119000101	TF041-TH-PWA;PWA-A790 M/B CLO	
411119000102	TF041-TH-PWA;PWA-A790 M/B CLO	
316119000029	TF041-TH-PCB;PWA-A790 M/B CLO	R00
271061330311	TF041-TH-RES;33 ,1/16W,5% ,	R1
796119070045	TF041-DOUBLE TAPE;MB TRANS BD	
791941190128	TF041-MECHANICAL KIT;COMMON,A	
242600000651	TF041-LABEL;25*10MM,3020F	
422118200013	TF041-TH-CABLE ASSY;2P,LED BD	
422118200021	TF041-TH-CABLE ASSY;LED TO MB	
422118200001	TF041-TH-CABLE;FLAT,1.0MM,40W	
796119030073	TF041-BRKT;COVER CHASSIS,A-79	
796119018001	TF041-BKT;EMI,VGA CABLE,A-790	
797215203024	TF041-NUT;M3,HEX,SUS,PSV	
796119061006	TF041-RUBBER SPONGE;18.9*14.5	
345118200001	TF041-GASKET;VGA BRACKET,A770	
345114900001	TF041-GASKET;USB CON1,9X3.5X1	
796119070014	TF041-DUO-PAK,DP-420,OFF-WHIT	
795941130002	TF041-CORE;FERRITE CORE + ADH	
791911190103	TF041-PWA;PWA-A790,I/O BD,W/	
411119000001	TF041-TH-PWA;PWA-A790,I/O BD	
411119000002	TF041-TH-PWA;PWA-A790,I/O BD	
331040080005	TF041-TH-CON;HDR,MA,20P*4,1.2	J2
331040060012	TF041-TH-CON;HDR,MA,15P*4,1.2	J7
411119000003	TF041-TH-PWA;PWA-A790,I/O BD	
272101016401	TF041-TH-CAP;1U ,CR,10V,10%	2000,C2001,C3,C501,C502C503,C

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Part Number	Deacription	Location(S)
272001106404	TF041-TH-CAP;10U,6.3V ,10%,08	C4,C554,C605
272105270305	TF041-TH-CAP;27P ,50V ,5%,04	C2002,C2003,C516,C540
272071475403	TF041-TH-CAP;4.7U,6.3V,10%,06	531,C532,C537,C552,C562C584,C
272431157520	TF041-TH-CAP;150U,KOCAP,6.3V,	C594
272030102411	TF041-TH-CAP;1000P,2KV,10%,18	618,C619,C646,C647,C648
272013106504	TF041-TH-CAP;10U,25V,+/-20%,1	C628,C630,C649
272105471408	TF041-TH-CAP;470P ,50V,10%,04	C629,C631
272105101313	TF041-TH-CAP;100P ,50V ,5%,04	635,C636,C637,C638,C639C640,C
272101015402	TF041-TH-CAP;1U,6.3V,+/-10%,04	C645,C651,C652
272105470403	TF041-TH-CAP;47P ,50V ,+/-10	511,C512,C522,C650,C653C654,C
288100541004	TF041-TH-DIODE;BAT54ALT1,COM.	D2,D501
288100056022	TF041-TH-DIODE;BAW56,70V,215m	504,D505,D506,D507,D508
288100054034	TF041-TH-DIODE;BAT54,30V,200m	D509
288100099015	TF041-TH-DIODE;BAV99,70V,450M	510,D511,D512,D513,D525
288100112005	TF041-TH-DIODE;EC11FS2-TE12L,	D516
288104148020	TF041-TH-DIODE;RLS4148,200MA,	D519
295000010218	TF041-TH-FUSE;FAST,2A,63VDC,1	F1,F501,F506
295000010213	TF041-TH-FUSE;0.14A/60V,POLY	F505
291000011809	TF041-TH-CON;HDR,FM,90P*2,.8M	J1
291000016034	TF041-TH-CON;HDR,MA P=0.5,H=1	J3
291000025204	TF041-TL-CON;D,MA,52P,.635MM,	J4
291000255201	TF041-TH-CON;MINI PCI-EXPRESS	J6
291000410208	TF041-TL-CON;WFR,MA,2P,1.25,S	J10,J20
291000154019	TF041-TH-CON;FPC/FFC,40P,.7MM	J12
291000011227	TF041-TL-CON;WFR,MA,12P,1.25M	J15

Part Number	Deacription	Location(S)
291000411504	TF041-TL-CON;WFR,MA,15P,1.25V	J18
291000015207	TF041-TL-CON;HDR,FM,P=1.0,H=2	J501
291000011237	TF041-TH-CON;HDR,FM P=0.5 H=4	J502,J503,J504
273000500182	TF041-TH-CHOKE COIL;120OHM/10	L516,L517,L518,L519
272075100310	TF041-TH-CAP;10P ,CR,50V ,5%	C501,PC502,PC503,PC513,C514,P
272075104710	TF041-TH-CAP;0.1U ,50V,+80-2	C504,PC506,PC508,PC509,C511,P
288105252004	TF041-TH-DIODE;MMSZ5252B,24V,	PD1,PD501
288100034012	TF041-TH-DIODE;SSA34,40V,3A,S	D1,PD502,PD503,PD504
273000150354	TF041-TH-FERRIET CHIP;120OHM/	PL502,PL503,PL504
288206679005	TF041-TH-TRANS;FDS6679_NL,P-M	PQ502
288200144030	TF041-TH-TRANS;DDTC144TKA,N-M	Q2
288227002024	TF041-TH-TRANS;2N7002LT1,N-CH	Q501,Q503,Q504,Q512
288200144029	TF041-TH-TRANS;DTC144WK,NPN,S	502,Q505,Q508,Q510,Q513Q514
288200069011	TF041-TH-TRANS;BCP69,PNP,SOT-	Q506,Q511
288200351007	TF041-TH-TRANS;NDS351-NL,N-MO	Q507
271621822306	TF041-TH-RP;8.2K*8,10P,1/32W,	RP501,RP502,RP503
271611103305	TF041-TH-RP;10K*4 ,8P ,1/16W,	RP506,RP508
271061205101	TF041-TH-RES;2M ,1/16W,1% ,	R3
271061152502	TF041-TH-RES;1.5K ,1/16W,5% ,	R4
271061103307	TF041-TH-RES;10K ,1/16W,5% ,	2001,R2002,R2003,R5,R57,R580,I
271061822307	TF041-TH-RES;8.2K ,1/16W,5% ,	502,R505,R506,R507,R508R509,R
271061102310	TF041-TH-RES;1K ,1/16W,5% ,	503,R504,R514,R515,R518R524,R
271061104306	TF041-TH-RES;100K ,1/16W,5% ,	522,R660,R783,R796,R797R798,R
271061101109	TF041-TH-RES;100 ,1/16W,1% ,	R523
271061593102	TF041-TH-RES;59K ,1/16W,1% ,	R537

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Part Number	Deacription	Location(S)
271061333304	TF041-TH-RES;33K ,1/16W,5% ,0	R541
271061000003	TF041-TH-RES;0 ,1/16W,0402	550,R553,R555,R558,R559R611,R
271061393103	TF041-TH-RES;39K ,1/16W,1% ,0	609,R610,R662,R663,R664R665,R
271061472312	TF041-TH-RES;4.7K ,1/16W,5% ,	513,R542,R556,R626,R630R672,R
271061201107	TF041-TH-RES;200 ,1/16W, 1%,	R635
271061330311	TF041-TH-RES;33 ,1/16W,5% ,	R600
271061122104	TF041-TH-RES;1.24K ,1/16W, 1	R726
271071499215	TF041-TH-RES;49.9,0603,1%,1/1	729,R730,R733,R734,R737R738,R
271061105307	TF041-TH-RES;1M ,1/16W,5% ,	R2000,R782
271061474304	TF041-TH-RES;470K ,1/16W,5% ,	R769,R781
271061750105	TF041-TH-RES;75,1/16W,1%,0402	R792,R793,R794,R795
271061331313	TF041-TH-RES;330,1/16W,5% ,04	R802,R803
286301022001	TF041-TH IC;ADM1022ARQ QSOP-1	U1
284583628004	TF041-TH-IC;ISA BRIDGE,W83628	U501
284583629004	TF041-TH-IC;ISA BRIDGE,W83629	U509
282574125015	TF041-TH-IC;SN74AHCT125PWR,QU	U511
284510268002	TF041-TH-IC;SIO10N268,SMSC SU	U512
284505752007	TF041-TH-IC;BCM5752;GIGA Bit	U514
286302506002	TF041-TH-IC;MIC2506YM,USB PWR	U517
286303311001	TF041-TH-IC;ADM3311EARU TSSOP	U518,U522
273001050206	TF041-TL-XSFORMER;100/1000 BA	U519
281300732013	TF041-TH-IC;NC7S32,SINGLE OR	U520
282574164008	TF041-TH-IC;74VHC164,SIPO REG	U521
282053306002	TF041-TH- IC;PI5C3306,2 BIT B	U523
284501284006	TF041-TH-IC;PACSZ1284-02QR,QS	U524

Part Number	Deacription	Location(S)
288100006006	TF041-TH-DIODE ARRAY;PACDN006	U525
274012500430	TF041-TH-XTAL;25MHZ,30PPM,18P	X501
316119000001	TF041-TH-PCB;PWA-A790,I/O BD	R01
242600000673	TF041-LABEL;26.5*4MM,HI-TEMP,	
242600000654	TF041-LABEL;27*7MM,HI-TEMP 26	
242600000572	TF041-LABEL;4*3MM,HI-TEMP,260	
282074212002	TF041-TH-IC;SN74LVC2G125,DUAL	U502,U504
272011226706	TF041-TH-CAP;22U ,CR,10V,1206	C524,C613
273000150374	TF041-TH-FERRITE CHIP;120OHM/	1500,L2000,L2001,L42,L51,L502,I
288101005003	TF041-TH-DIODE ; ESD. V-PORT-	517,D518,D520,D521,D522D523,I
291000410804	TF041-TL-CON;WFR,MA,8P*1,1.25	J17
271611750302	TF041-TH-RP;75*4 ,8P ,1/16W,	RP509
288202303008	TF041-TH-TNANS;SI2303,P-MOSFE	Q1
273000610054	TF041-TH-FERRITE ARRAY;120OHM	FA501,FA502
271045107104	TF041-TH-RES;01 ,1W ,1% ,2	PR501
291000010629	TF041-TH-CON;HDR,MA,6P,1.25mm	J11
282153160001	TF041-TH- IC;TS5A3160DBVR,ANA	U503,U507,U508
273000500189	TF041-TH-CHOKE COIL;90OHM/100	L533,L534
271071000312	TF041-TH-RES;0 ,1/16W,5% ,	R775
271611102308	TF041-TH-RP;1K*4 ,8P ,1/16W,	RP504
271061471308	TF041-TH-RES;470 ,1/16W,5% ,	R1
272105222504	TF041-TH-CAP;2200P,50V,+ -20%,	C1,C2
295000010243	TF041-TH-FUSE;NANO,10A/125V,R	PF501
288110150431	TF041-TH-TVS DIODE ; AZ1015-0	D514,D515
283460000020	TF041-TH-IC;FLASH,AT45DB041B,	U513

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Part Number	Deacription	Location(S)
796119011001	TF041-S-STANDOFF;M2,H=4.5MM,A	H21,H22
796119011002	TF041-S-STANDOFF;M2,H=9MM,A-7	H19,H20,H21,H22
796119040001	TF041-SPACER;H=4MM,M2*0.4,A-7	H2,H3,H4,H5
796115040005	TF041-SPACER;H=3.0MM,M2.0X0.4	H14,H15
796119052005	TF041-MYLAR;HDD-IO BD,A790	
796119052006	TF041-MYLAR;BAY-2,I/O,A-790	
796119042004	TF041-SPRING;POWER,ESD,A-790	SP1
796119042005	TF041-SPRING;MODEM,ESD,A-790	SP3
796119050007	TF041-MYLAR TAPE;8mm,YELLOW,M	
796114940001	TF041-STAND OFF;M2 L2 D5,ML90	H10,H6
375102030012	TF041-NUT-HEX;M2,2,NIW	H19,H20,H21,H22,H30,H31
797616422045	TF041-S-STANDOFF;M2L4*5,NIW,N	H17
291000000818	TF041-TH-CON;USB,FM,4P*2,R/A,	J9
331510080009	TF041-CON;RBN,MA,80P,,635MM,R	J13
291000811501	TF041-TH-CON;PHONE,JACK,JM34F	J14
331040015004	TF041-TH-CON;D,FM,15P,2.29,R/	J16
331040025003	TF041-TH-CON; D,FM,25P,2.77,R	J19
331040009005	TF041-TH-CON;D,MA,9P,2.775,R/	J21
331000004089	TF041-CON;BATTERY,0402A120,4P	PJ1
791911190124	TF041-DDR2 ASSY;(5D5)A790,533	
323711600001	TF041-DDR2 SODIMM MODULE,512M	
791911190145	TF041-BATTERY ASSY;A790,(B),	
338911120029	TF041-BATTERY PACK;LI,11.1V/9	
441118000004	TF041-BATT ASSY;11.1V/9.6AH,L	Spec-R0D
225686920001	TF041-TAPE;INSULATING,POLYEST	

Part Number	Deacription	Location(S)
225686920002	TF041-TAPE;ADHENSIVE,DOUBLE-F	
242118000008	TF041-LABEL;BATTERY,12.5V/9.6	
242683200024	TF041-LABEL;5*20,BLANK,COMMON	
242686000009	TF041-LABEL;LOT NUMBER,HOOK	
242687600004	TF041-LABEL;MIRRIR PAPER,WHIT	
338937010065	TF041-BATTERY;LION,3.7V,2400m	
342118000002	TF041-CONTACT PLATE;W4L25T0.1	
342118000004	TF041-CONTACT PLATE;W5L36T0.1	
342120100001	TF041-CONTACT PLATE;W5L58T0.1	
342680900016	TF041-CONTACT PLATE;W5L102T0.	
342686000018	TF041-CONTACT PLATE;W4L63T0.1	
342801200002	TF041-CONTACT PLATE;W5L27T0.1	
344118000012	TF041-COVER;BATTERY,A770-PRI,	
344118000013	TF041-HOUSING;BATTERY,A770-PR	
346118000010	TF041-INSULATOR;FIBRE,BATT,5	
346118000016	TF041-INSULATOR;FIBRE,BATT,2	
346801200001	TF041-INSULATOR;5,BATTERY ASS	
361400004013	TF041-ADHESIVE;ABS+PC PACK,G4	
411118000225	TF041-PWA;PWA-A770PRI/BATT,LI	
295000100009	TF041-FUSE;228R,139C',5A/250V	F1
331000007071	TF041-CON;BATT,FEMALE,7PIN,2.	CON1
332100020022	TF041-WIRE;#20,UL1007,45mm,BL	B-
332100020033	TF041-WIRE;#20,UL1007,22mm,BL	P-
332100026021	TF041-WIRE;#26,UL1007,152MM,B	VH
332100026043	TF041-WIRE;#26,UL1007,140mm,O	VL

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Part Number	Deacription	Location(S)
332100026044	TF041-WIRE;#26,UL1007,30mm,OR	SMD
332100026045	TF041-WIRE;#26,UL1007,30mm,BL	SMC
332110020193	TF041-WIRE;#20,UL1007,45MM,RE	B+,P+
361400003017	TF041-JET-MELT ADHESIVES;3478	
365350000009	LF-SOLDER WIRE;SN96.5/AG3.0/C	
411118000226	TF041-PWA;PWA-A770PRI/BATT,LI	
271071100103	TF041-TH-RES;10 ,1/16W,1% ,	R24,R7
271071101107	TF041-TH-RES;100 ,1/16W,1% ,	14,R15,R16,R17,R19,R2,R1,R28,R
271071104114	TF041-TH-RES;100K ,1/16W,1% ,	R13
271071104310	TF041-TH-RES;100K ,1/16W,5% ,	R12,R8
271071105312	TF041-TH-RES;1M ,1/16W,5% ,	R1,R18,R20,R3
271071502304	TF041-TH-RES;5K ,1/16W,5% ,	R5,R6
271071613101	TF041-TH-RES;61.9K,1/16W,1% ,	R10,R23
271071842101	TF041-TH-RES;8.45K,1/10W,1% ,	R22
272001475412	TF041-TH-CAP;4.7U,10V,10%,080	C8
272003105402	TF041-TH-CAP;1U ,CR,25V ,10	C9A,C9B
272003474403	TF041-TH-CAP;47U ,CR,25V,10%	C3
272003475401	TF041-TH-CAP;4.7U,25V,10%,080	C5
272005105402	TF041-TH-CAP;0.1U,CR,50V,10%,	C1,C2
272072474403	TF041-TH-CAP;0.47U,16V,10%,06	C12,C4,C9
272073104712	TF041-TH-CAP;0.1U,25V,10%,060	13,C14,C15,C16,C19,C20,21,C22,
272073105403	TF041-TH-CAP;1U, CR, 25V ,10%	C18
272075151309	TF041-TH-CAP;150P ,50V ,5% ,0	C11
272075222407	TF041-TH-CAP;2200P,50V ,10%,0	C7
272075680307	TF041-TH-CAP;68P ,50V ,5% ,0	C10,C6

Part Number	Deacription	Location(S)
286002084002	TF041-TH-IC;BQ2084,GAS GAUGE,	U1 V1.41
286029312002	TF041-TH-IC;BQ29312,PROTECTIO	U2
288100056026	TF041-TH-DIODE;UDZ5V6B-F,ZENE	ZD3,ZD4
288104148022	TF041-TH-DIODE;1N4148WS,75V,2	D1,D2
288204409003	TF041-TH-TRANS;AO4409,P-MOSFE	Q1,Q2,Q3,Q4
316118000048	TF041-PCB;PWA-A770/BATT-BD,PR	R0D
271046407105	TF041-TH-RES;0.040,2W,1%,2512	R9C,R9E,R9F
288100018007	TF041-TH-DIODE;PSD18C,TVS,18V	ZD7,ZD8
361200003204	TF041-SOLDER PASTE;PF606-P;FO	
242804400010	TF041-TH-LABEL;BAR CODE,20*5,	
288104024001	TF041-TH,DIODE,TVS ARRAY;40PF	ZD6
310111103045	TF041-THERMISTOR;10K,1%,BN35-	RT1
361200003201	TF041-ADHESIVE;SILICONE,DOW C	
346118000012	TF041-INSULATOR;25X80mm,FOR A	
346118000019	TF041-INSULATOR;FIBRE,24X59,F	
242118000009	TF041-LABEL;BLANK,BLACK,FOR A	
345118000005	TF041-RUBBER;CR,L20W7mm,T=2.0	
335152000171	TF041-FUSE;LR4-730F,POLY SWIT	
335152000134	TF041-FUSE;THERMAL FUSE,G7F51	
332100020040	TF041-WIRE;#20,UL1007,80mm,BL	
342680800002	TF041-CONTACT PLATE;W4L12T0.1	
346680900031	TF041-INSULATOR;BATT ASSY,THE	
461802300005	TF041-PACKING KIT;8350MP/6.6A	
221680820005	TF041-CARTON;BATTERY,CAIMAN,P	
221680850002	TF041-PARTITION;BATTERY,MARLI	

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Part Number	Deacription	Location(S)
221680850003	TF041-PARTITION;TOP/BTM,BATTE	
226687620001	TF041-SPONGE;320*290*10,CAIMA	
224801530001	TF041-PALLET;PLYWOOD,L1140*W1	
242679400008	TF041-LABEL;BAR CODE,NEW,COMM	
242686900045	TF041-LABEL;BLANK,55*25,OUTER	
225600020010	TF041-PE FILM;SKIN,PACKING	
225600020006	TF041-TAPE;CARTON,2.5W,30M/RL	
225600020002	TF041-TAPE;1/2",WRINKLE TAPE	
796119000003	TF041-DOOR;BATTERY KIT,A-790	
796119010003	TF041-COVER SCREW;A-790	
796119060007	TF041-RUBBER;BATTERY,A-790	
791911190133	TF041-HDD ASSY;(P8B)A790,STD,	
346112200015	TF041-GASKET;41*21*3.7M/M,A32	
346118200001	TF041-GASKET;93*5*5M/M,A770-H	
796119010002	TF041-SHOULDER SCREW;A-790	
796119051003	TF041-MYLAR;HDD,A-790	
796119051006	TF041-SPACER;PCB,DS,PITCHING	
796119060203	TF041-RUBBER;HDD,IP54,A-790	
796119061032	TF041-SPONGE;9 0*10.5*6,TOSHI	
796119061033	TF041-SPONGE;104*7.2*2,TOSHIB	
796119061034	TF041-SPONGE;25*19*3,TOSHIBA	
796119061035	TF041-SPONGE;TOSHIBA 6025GAS	
796119061036	TF041-SPONGE;9*7.2*4,,TOSHIBA	
796119061037	TF041-SPONGE;104*7.2*3,TOSHIB	
796119040002	TF041-EMI SPRING;HDD,A-790	

Part Number	Deacription	Location(S)
412119000004	TF041-TH-PWA ASSY;A790 IDE HD	
523450283088	TF041-HDD DRIVE; 80G, 2.5", I	
796119000005	TF041-CASE;HDD KIT,A-770	
796119010012	TF041-COVER;HDD,SUS,A770	
791911190151	TF041-INT WLAN OPTION;A790,(W	
412600000056	TF041-PCB ASSY;WLAN CARD;WM39	
313002000262	TF041-ANTENNA;WIRELESS+BT 12.	
313002000263	TF041-ANTENNA;WIRELESS 12.1"R	
796119072006	TF041-LABEL;INTEL CENTRINO DU	
796116078002	TF041-LABEL;WLAN FCC,M230 & A	
791911190160	TF041-FINGERPRINT ASSY;A790,	
411119000044	TF041-TH-PWA;PWA-A790 FINGER	
411119000103	TF041-FINGER PRINT KIT VFS131	
328000101001	TF041-FLEX FINGER PRINT VFS10	J500
411119000046	TF041-TH-PWA;PWA-A790 FINGER	
271061000003	TF041-TH-RES;0 ,1/16W,0402	R3
272101016401	TF041-TH-CAP;,1U ,CR,10V,10%	10,C13,C14,C15,C18,C19,5,C64
272103103407	TF041-TH-CAP;0.01U ,CR,25V ,1	C11
271061203112	TF041-TH-RES;20K ,1/16W,1% ,	R14,R15
271061220308	TF041-TH-RES;22 ,1/16W,5% ,	R10,R9
271061101109	TF041-TH-RES;100 ,1/16W,1% ,	R11,R13
271061490102	TF041-TH-RES;49.9 ,1/16W,1% ,	R6
271061152502	TF041-TH-RES;1.5K ,1/16W,5% ,	R5
271061240102	TF041-TH-RES;24.9,1/16W,1% ,0	R4
272105180308	TF041-TH-CAP;18P ,50V ,+/-5%	C8,C9

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Part Number	Decription	Location(S)
273000500183	TF041-TH-FERRITE CHIP;120OHM/	L2
274011200416	TF041-TH-XTAL;12M,30PPM,16PF,	Y1
286307046002	TF041-TH-IC;UHS DUAL INVERTER	U3,U5
316119000013	TF041-TH-PCB;PWA-A790 FINGER	R01
271061105307	TF041-TH-RES;1M ,1/16W,5% ,	R12,R16,R8
273000990446	TF041-TH-INDUCTOR;1UH,MLL-160	L3,L4,L5
272071225406	TF041-TH-CAP;2.2U ,CR,6.3V ,1	C12,C16
272075680307	TF041-TH-CAP;68P ,50V ,5% ,0	C17,C20,C21
291000151007	TF041-TH-CON;FFC/FPC R/A P=0.	J2
271061155103	TF041-TH-RES;1.5M,1/16W,1%,04	R7
288105105001	TF041-TH-STEERING DIODE;PSR05	D1
422119000013	TF041-CABLE ASSY I/O TO FINGE	
796119090003	TF041-COVER;CHASSIS,A770-A790	
796119061049	TF041-RUBBER;IO BD-COVER CHAS	
422121200016	TF041-CABLE ASSY;POWER TO FNK	
796119070030	TF041-GASKET;FINGER PRINT,A79	
796119070031	TF041-GASKET;FINGER PRINT BAC	
797416404000	TF041-WASH;M2,FLT,STD,FE,NIW	
796119000010	TF041-BRKT;FINGER PRINT KIT,A	
796119050100	TF041-BRKT;FINGER PRINT,A790	
565111900003	TF041-S/W;CD ROM,FPAP PCV100,	
791911190171	TF041-BAY1 OPTION;A790,(A)CD-	
242600000653	TF041-LABEL;MODEL,5M,MITAC	
791941182250	TF041-S/W;CD-ROM UTIL,TEAC	
551102200018	TF041-DISKETTE;FLOPPY,1.44M,3	

Part Number	Decription	Location(S)
242600000652	TF041-LABEL;3.5"DISKETTE,BLAN	
795911820001	TF041-CD ROM;TEAC CD-224E-N93	
791941190202	TF041-CANISTER;CD-ROM,A790	
796119051018	TF041-COVER;CDROM 24X,A-SERIE	
796119090013	TF041-HOLDER;BAY1,A-790	
242600000651	TF041-LABEL;25*10MM,3020F	
242600000653	TF041-LABEL;MODEL,5M,MITAC	
796119069002	TF041-RUBBER PAD;30*5*1.5T,A-	
796119061005	TF041-RUBBER PAD;L43*W10*T4.5	
411119000068	TF041-TH-PWA;PWA-A790 BAY1 CD	
316119000020	TF041-TH-PCB;PWA-A790 BAY1 CD	
331040060013	TF041-TH-CON;HDR,15P*4,FM,1.2	J1
291000015058	TF041-TH-CON;HDR,MA,25P*2,.8M	J2
797215202016	TF041-NUT;M2,HEX,SUS,PSV	
242600000572	TF041-LABEL;4*3MM,HI-TEMP,260	
796118270004	TF041-CU FOIL;BAY1 CD-ROM,7.5	
796118200005	TF041-CU FOIL;BAY1 CD-ROM, 13	
791911190190	TF041-BAY2 OPTION;A790,(0)NO	
791941182220	TF041-DOOR ASSY;BAY2,STANDARD	
796119010002	TF041-SHOULDER SCREW;A-790	
796119010001	TF041-DOOR HINGE;SUS,A-790	
796119032011	TF041-DOOR;BAY2,SUS PIN,A-790	
796119060202	TF041-RUBBER;BAY2,IP54,A-790	
796119060029	TF041-RUBBER;LCD PLUG,A-790	
796119060030	TF041-RUBBER;PLUG,LCD BUMPER,	

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Part Number	Deacription	Location(S)
791911190210	TF041-EXP/C-BAG/PACK;A790-7,(	
791941182240	TF041-PACKING;W/O CARRING,A77	
242600000652	TF041-LABEL;3.5"DISKETTE,BLAN	
242600000651	TF041-LABEL;25*10MM,3020F	
796115070064	TF041-LABEL;110MM*85MM,PACKIN	
798961149110	TF041-PE BAG;#10,240*340 mm,M	
798961150014	TF041-PE BAG;ANTI-STATIC,450*	
798961190101	TF041-PE BAG;140*200*0.1mm,A7	
798961190201	TF041-BOX;BATTERY,A790	
798961190003	TF041-CARTON;NB,W/O CARRYING	
798961190301	TF041-END CAP;MAIN UNIT,R&L,A	
796114978002	TF041-MYLAR;TRANSPARENT,290*2	
225600020006	TF041-TAPE;CARTON,2.5W,30M/RL	
222600040006	PE FILM;SKIN,PACKING;W/LETTER	
221686050015	TF041-REINFORCE BRKT;L1000*50	
221804950002	TF041-REINFORCE BRKT;830x50x5	
221686050014	TF041-REINFORCE BRKT;L1200*50	
225000020001	TAPE;1/2",LIMPID,20YARD/REEL,	
225600020005	TF041-TAPE;AC04,FOR CG,COMMON	
225600020008	TF041-TAPE;T=0.05MM,W=20MM,KA	
224672330002	TF041-PALLET;1200x1050x104MM,	
791941190114	TF041-ACCESSORY KIT;(S)A790,U	
791921160005	TF041-AC ADAPTER ASSY; 90-264	
422118200003	TF041-TH-CABLE ASSY;AUDIO EMI	
332810018001	TF041-PWR CORD;125V,10A,3P,PV	

Part Number	Deacription	Location(S)
796119072001	TF041-LOGO;FRONT,A-790	
796119072002	TF041-LOGO;FACE,A-790	
422118200017	TF041-TH-CABLE ASSY;LAN,2P,CA	
565111900001	TF041-S/W;CD ROM,SYSTEM DRIVE	
796119059012	TF041-LABEL;SAFETY/EMC,A790,M	
799001190007	TF041-Manual;Quick Start Guid	
421600000049	TF041-CABLE ASSY;PHONE LINE,6	
795941130003	TF041-CORE;FERRITE CORE,FH30*	
230000030047	TF041-RIBBON;13CM*300M,LABEL	
230000030048	TF041-RIBBON;11CM*300M,PT800	
791911190075	TF041-TOUCH PAD ASSY;A790,STD	
442119000001	TF041-TOUCHPAD MODULE;TM61PUG	
796115050035	TF041-PLATE_TP_ALPS_M220	
796119061046	TF041-RUBBER SPONGE;49*4*3.5t	
422119000051	TF041-FFC;P=0.5,12PIN,TRACK P	
411119000029	TF041-TH-PWA;PWA-A790,TOUCH P	
411119000030	TF041-TH-PWA;PWA-A790,TOUCH P	
411119000031	TF041-TH-PWA;PWA-A790,TOUCH P	
291000410409	TF041-TL-CON;HDR 4P,MA,SHROUD	SJ501
271061103307	TF041-TH-RES;10K ,1/16W,5% ,	SR501,SR502
272001106404	TF041-TH-CAP;10U,6.3V ,10%,08	SC501
272101016401	TF041-TH-CAP;1U ,CR,10V,10%	SC502
242600000572	TF041-LABEL;4*3MM,HI-TEMP,260	
316119000010	TF041-TH-PCB;PWA-A790,TOUCH P	R01
291000151219	TF041-TH-CON;FPC/FFC,12P,0.5M	SJ502

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9. Spare Parts List - 21

[illegible]

Reference Material

❖ Intel Yonah Processor	Intel. INC
❖ 945GM North Bridge Intel	Intel. INC
❖ Intel ICH7-M South Bridge	Intel. INC
❖ System Explode View	Technology.Corp /MiTAC
❖ Hardware Engineering Specification	Technology.Corp /MiTAC

SERVICE MANUAL FOR A790

Sponsoring Editor : Ally Yuan

Author : Irene.Yu

Publisher : MiTAC Technology Corp.

Address : No.269, Road 2, Export Processing Zone, Kunshan, P.R.C

Tel : 086-512-57367777

Fax : 086-512-57385099

First Edition : Mar.2007

E-mail : Ally.Yuan @ mic.com.tw

Web : <http://www.mitac.com>

<http://www.mtc.mitacservice.com>
